

IN THE UNITED STATES DISTRICT COURT  
FOR THE DISTRICT OF DELAWARE

POWER INTEGRATIONS, INC.,	)	<b>REDACTED</b>
	)	<b>PUBLIC VERSION</b>
Plaintiff,	)	
	)	
v.	)	C.A. No. 04-1371-JJF
	)	
FAIRCHILD SEMICONDUCTOR	)	
INTERNATIONAL, INC., and FAIRCHILD	)	
SEMICONDUCTOR CORPORATION,	)	
	)	
Defendants.	)	

**COMBINED APPENDIX TO DEFENDANTS': (i) OPENING POST-TRIAL BRIEF  
IN SUPPORT OF THEIR ASSERTION THAT THE PATENTS-IN-SUIT  
ARE UNENFORCEABLE DUE TO INEQUITABLE CONDUCT; AND  
(ii) PROPOSED FINDINGS OF FACT AND CONCLUSIONS OF LAW  
REGARDING THE UNENFORCEABILITY OF THE PATENTS-IN-SUIT  
DUE TO INEQUITABLE CONDUCT**

(VOLUME II of V)

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Menlo Park, CA 94025  
(650) 614-7400

Dated: November 5, 2007

**TABLE OF CONTENTS**

**VOLUME I**

DX 17, Electronic Design, Volume 38, No. 6 (March 22, 1990)

DX 55, International Electron Devices Meeting, December 5-7, 1983

DX 56, International Electron Devices Meeting, December 13-15, 1982

DX 59, Physics and Technology of Power MOSFETs, A Dissertation Submitted to the Department of Electrical Engineering and the Committee on Graduate Studies of Stanford University in Partial Fulfillment of the Requirements for the Degree of Doctor of Philosophy, Shi-Chung Sun (February 1982)

DX 69, Seventh Annual Applied Power Electronics Conference and Exposition, February 23-27, 1992

DX 70, PWR-SMP240, PWM Power Supply IC, 85-265 VAC Input, Isolated, Regulated DC Output

DX 74, PWR-SMP260, PWM Power Supply IC, 85-265 VAC Input, Isolated, Regulated DC Output

DX 76, SMP211, PWM Power Supply IC, 85-265 VAC Input, Isolated, Regulated DC Output

DX 77, PWR-SMP3, PWM Power Supply IC, 120 VAC Input, Isolated, Regulated DC Output

DX 89, United States Patent No. 4,626,879

DX 90, PIF 129750-129777

**VOLUME II**

DX 91, PIF 129301-129321

DX 100, Prosecution History, FCS0000015-114

DX 102, Prosecution History, FCS0000122-206

DX 104, Prosecution History, FCS0000226-316

DX 106, Prosecution History, FCS0000336-477

**VOLUME III**

DX 110, PIF17419

DX 113, Invention Disclosure Form, PIF 63314-24

DX 114, Project PS03 Index, 3/28/90, PIF 129325-46

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DX 116, Project SMP1A Index, 3/27/90, PIF 129389-410

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DX 118, PIF 129449-51

DX 119, PIF 129454-84

DX 120, SMP212/220 Task List, 8/14/92, PIF 129499-504

DX 121, PWR-SMP212, PWM Power Supply IC, 85-265 VAC Input, Isolated, Regulated DC Output

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DX 126, PWR-SMP240, PWM Power Supply IC, 85-265 VAC Input, Isolated, Regulated DC Output

DX 192, United States Patent No. 5,146,298

DX 472, FCS1685956-93

DX 600, Optimum Design of Power MOSFETS, P.L. Hower, T.M.S. Heng and C. Huang, Unitrode Corporation, Watertown, Mass. 02171

DX 601, United States Patent & Trademark Office, Application No. 90/008,324

DX 602, United States Patent & Trademark Office, Application No. 90/008,327

DX 616, International Electron Devices Meeting, December 8-10, 1980

DX 617, International Solid-State Circuits Conference, February 18, 1981

DX 618, Process and Device Design of a 1000-Volt MOS IC

DX 619, Integrated Circuits for the Control of High Power, Robert S. Wrathall, David Tam, Louis Terry, Stephen P. Robb

DX 620, Integrated Power Devices, J. Tihanyi

DX 621, Journal of Solid-State Circuits, Vol. SC-15, No. 3, June 1980

DX 622, Integrated High and Low Voltage CMOS Technology

DX 623, International Solid-State Circuits Conference, February 18, 1981

DX 624, Lateral DMOS Transistor Optimized for High Voltage BIMOS Applications

DX 625, International Solid-State Circuits Conference, February 20, 1981

DX 626, Transactions on Electron Devices, FCS0526755-67

DX 627, High Voltage MOS Integrated Circuits, A Technology and Application Overview, KE001450-65

DX 628, KE001513-22

DX 629, KE001481-84

DX 633, Privilege Log for Klas Eklund documents

#### **VOLUME IV**

DX 1000, United States Patent No. 5,245,526

DX 1001, PWR-SMP211, PWM Power Supply IC, 85-265 VAC Input, Isolated, Regulated DC Output

DX 1002, PIF 129975-130008

DX 1003, Power Integrations' Responses and Objections to Defendants' Third Set of Requests for Admission (Nos. 44-50)

DX 1004, Form 10-Q, Filed 11/7/05 for Period Ending 9/30/05

DX 1005, International Electron Devices Meeting, December 3-5, 1979

DX 1006, Philips Journal of Research, Vol. 35, No. 1, March 13, 1980

DD1202

PX 1, United States Patent No. 6,249,879

PX 2, United States Patent No. 6,107,851

PX 3, United States Patent No. 6,229,366

PX 4, United States Patent No. 4,811,075

PX 8, PIF 00001-76

PX 19, Electronic Design, February 17, 1983, PIF 08765-70

PX 29, Klas Eklund notes

PX 30, Klas Eklund notes

PX 50, Letter to Alys Hay from Thomas Schatzel, KE 00012-14

PX 56, Technology License Agreement, PIF 23640-64

PX 272, 650V/1A, SPS 1-chip Process, FCS0176604-24

PX 325, Invention Disclosure Form, PIF 63306-13

PX 326, Invention Disclosure Form, PIF 63314-24

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## **VOLUME V**

Alex Djenguerian Deposition, 8/23/05

Klas Eklund Deposition, 10/14/05

**Klas Eklund Deposition, 6/7/07**

**James Go Deposition, 9/14/05**

**Leif Lund Deposition, 8/15/05**

**Leif Lund Deposition, 3/2/06**

**Thomas Schatzel Deposition, 9/15/05**

185623.1

**DX 91**

**REDACTED**



**DX 100**

## PATENT APPLICATION



09192959

10523 U.S. PTO

09/192959



11/16/98

INITIALS

H. J. J.

## CONTENTS

	Date received (incl. C. of M.) or Date Mailed		Date received (incl. C. of M.) or Date Mailed
1. Application <u>6</u> papers.		42.	
2. <u>IDS</u>	<u>11/16/98</u>	43.	
3. <u>CA</u>	<u>2-25-99</u>	44.	
4. <u>P/A assignee</u>	<u>5-20-99</u>	45.	
5. <u>Notice of Allowance</u>	<u>4/1/99</u>	46.	
10/13 <u>Reg (3 months)</u>	<u>10-10-00</u>	47.	
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11/13 <u>Notice of Allowance</u>	<u>1/30/01</u>	49.	
9. <u>5/1/00 Formal Drawings (6 sheets)</u>	<u>4/2/01</u>	50.	
10. <u>CA</u>	<u>3-19-01</u>	51.	
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Case No. 04-1371-JJFDEFT Exhibit No. DX 100


Date Entered \_\_\_\_\_

Signature \_\_\_\_\_

FCS0000015

713	501
Class	Subclass

ISSUE CLASSIFICATION

**PATENT NUMBER**  
**8249876**  
  
**8249876**

Q.I.P.E. 1 RM SCANNED <i>sc</i> O.A. <i>1901</i>	PATENT DATE JUN 19 2000
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SECTION	CLASS 39	SUBCLASS 51.4	ART UNIT 247	EXAMINER Butler
713		501	2182	FILED WITH: <input type="checkbox"/> OHSK (CRF) <input type="checkbox"/> FICHE

FEB 17 2012

## OF CORRECTION

**PREPARED AND APPROVED FOR ISSUE** **CERTIFICATE**

FEB 14 2002

ISSUING CLASSIFICATION										OF CORRECTION	
ORIGINAL			CROSS REFERENCE(S)								
CLASS		SUBCLASS	CLASS		SUBCLASS (ONE SUBCLASS PER BLOCK)						
713		501	713		300	503					
INTERNATIONAL CLASSIFICATION											
60	6	F			1	04					

☐ Continued on Issue Slip Inside File Jacket

<input type="checkbox"/> <b>TERMINAL DISCLAIMER</b>	<b>DRAWINGS</b>			<b>CLAIMS ALLOWED</b>	
	Sheets Draw. <div style="text-align: center;">6</div>	Figs. Draw. <div style="text-align: center;">6</div>	Print Fig. <div style="text-align: center;">1</div>	Total Claims <div style="text-align: center;">32</div>	Print Claim for O.G. <div style="text-align: center;">11 ✓</div>
<input type="checkbox"/> a) The term of this patent subsequent to _____ (date) has been disclaimed.  <input type="checkbox"/> b) The term of this patent shall not extend beyond the expiring date of U.S. Patent No. _____	_____ (Assistant Examiner) (Date)			<b>NOTICE OF ALLOWANCE MAILED</b>	
	<div style="text-align: center;"> <b>Dennis M. Butler</b>  <b>Primary Examiner</b> </div> <div style="text-align: center;"> <i>Dennis M. Butler</i>      6-27-91          (Primary Examiner)      (Date)       </div>			<div style="text-align: right;">1:30-01</div> <div style="text-align: center;"> <b>ISSUE FEE</b>      CN       </div> <div style="display: flex;"> <div style="flex: 1;">         \$ Amount Due  <div style="text-align: center;">1240.00</div> </div> <div style="flex: 1;">         Date Paid  <div style="text-align: center;">5-1-01</div> </div> </div>	
<input type="checkbox"/> c) The terminal _____ months of this patent have been disclaimed.	<div style="text-align: center;"> <i>[Signature]</i>          (Legal Representative [Signature])       </div>			<div style="text-align: center;"> <b>ISSUE BATCH NUMBER</b>  <div style="text-align: center;">B25</div> </div>	
<b>WARNING:</b> The information disclosed herein may be restricted. Unauthorized disclosure may be prohibited by the United States Code Title 35, Sections 122, 181 and 368. Possession outside the U.S. Patent & Trademark Office is restricted to authorized employees and contractors only.					

Form PTO-035A  
(Rev. 5-2001)

FOR TITIAL DRAWINGS \_\_\_\_\_ (SHEET) SET \_\_\_\_\_  
(LABEL AREA)

**Save Fee In File**

**(FACE)**

FCS0000016

PATENT APPLICATION SERIAL NO. 09/192959

U.S. DEPARTMENT OF COMMERCE  
PATENT AND TRADEMARK OFFICE  
FEE RECORD SHEET

11/24/1998 DWTLE 00000010 09192959

01 FC:101	750.00 DP
02 FC:102	234.00 DP
03 FC:103	252.00 DP

PTO-1556  
(5/87)

U.S. OFFICE OF PATENT AND TRADEMARKS

FCS0000017

SERIAL NUMBER 09/192,959	FILING DATE 11/16/98	CLASS 713	GROUP ART UNIT 2781	ATTORNEY DOCKET NO. 10256/003001
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**APPLICANT**  
BALU BALAKRISHNAN, SARATOGA, CA; ALEX DZIEWURRIAN, SARATOGA, CA; LEIF LUND, SAN JOSE, CA.

**\*\*CONTINUING DOMESTIC DATA\*\*\*\*\***  
VERIFIED  
DMB none

**\*\*371 (MAT'L STAGE) DATA\*\*\*\*\***  
VERIFIED  
DMB none

**\*\*FOREIGN APPLICATIONS\*\*\*\*\***  
VERIFIED  
DMB none

IF REQUIRED, FOREIGN FILING LICENSE GRANTED 12/02/98

Foreign Priority claimed 35 USC 118 (a)-(c) conditions met	Draw <input checked="" type="checkbox"/> No <input type="checkbox"/> Draw <input checked="" type="checkbox"/> No <input type="checkbox"/> Met after Allowance	STATE OR COUNTRY CA	SHEETS DRAWING 6	TOTAL CLAIMS 34	INDEPENDENT CLAIMS 6
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Verified and Acknowledged DMB None

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LOS Angeles, CA 90025*

**TITLE**  
7/11  
FREQUENCY JITTERING CONTROL FOR VARYING THE SWITCHING FREQUENCY OF A POWER SUPPLY

FILING FEE RECEIVED \$1,246	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT NO. _____ for the following:	<input type="checkbox"/> All Fees <input type="checkbox"/> 1.16 Fees (Filing) <input type="checkbox"/> 1.17 Fees (Processing Ext. of time) <input type="checkbox"/> 1.18 Fees (Issue) <input type="checkbox"/> Other _____ <input type="checkbox"/> Credit _____
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FCS0000018

# FISH RICHARDSON P.C.

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Menlo Park, California  
94025

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650 322-0777

Web Site  
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November 16, 1998

Attorney Docket No.: 10256/003001

Box Patent Application  
Assistant Commissioner for Patents  
Washington, DC 20231

Presented for filing is a new original patent application of:

**Applicant:** BALU BALAKRISHNAN, ALEX DJENGUERIAN, LEIF LUND  
**Title:** FREQUENCY JITTERING CONTROL

Enclosed are the following papers, including all those required to receive a filing date under 37 CFR §1.53(b):

	Pages
Specification	14
Claims	6
Abstract	1
Declaration	2
Drawing(s)	6

## Enclosures:

- New disclosure information, including:  
Information disclosure statement, 1 page.  
PTO-1449, 1 page.  
References, 1 item.
- Postcard.

"EXPRESS MAIL" Mailing Label Number EL11051451704

Date of Deposit Nov. 16, 1998

86/91/11  
11/16/98  
014  
S. H. Fish  
Richardson  
1879-1998

BOSTON  
NEW YORK  
SILICON VALLEY  
SOUTHERN CALIFORNIA  
TWIN CITIES  
WASHINGTON, D.C.

9192959-111698

10523 U.S. PTO  
09/192959  
11/16/98

FCS0000019

FISH & RICHARDSON P.C.

**BOX PATENT APPLICATION**

November 16, 1998

Page 2

Basic filing fee	\$ 760.00
Total claims in excess of 20 times \$18.00	252.00
Independent claims in excess of 3 times \$78.00	234.00
Multiple dependent claims	0.00
Total filing fee:	\$ 1246.00

A check for the filing fee is enclosed. Please apply any other required fees or any credits to deposit account 06-1050, referencing the attorney docket number shown above.

If this application is found to be INCOMPLETE, or if a telephone conference would otherwise be helpful, please call the undersigned at 650/322-5070.

Kindly acknowledge receipt of this application by returning the enclosed postcard.

Please send all correspondence to:

Roger S. Borovoy  
Fish & Richardson P.C.  
2200 Sand Hill Road, Suite 100  
Menlo Park, CA 94025

Respectfully submitted,

  
Bao Q. Tran  
Reg. No. 37,955

Enclosures

0002.PALI

09192959.111698

FCS0000020

PATENT APPLICATION FEE DETERMINATION RECORD Effective November 10, 1998					Application or Docket Number <u>02739</u>	
<b>CLAIMS AS FILED - PART I</b>						
(Column 1)		(Column 2)				
FOR	NUMBER FILED	NUMBER EXTRA				
BASIC FEE						
TOTAL CLAIMS	24	minus 20 =		4		
INDEPENDENT CLAIMS	11	minus 3 =		8		
MULTIPLE DEPENDENT CLAIM PRESENT						
* If the difference in column 1 is less than zero, enter "0" in column 2						
<b>CLAIMS AS AMENDED - PART II</b>						
(Column 1)		(Column 2)		(Column 3)		
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA			
Total	32	Minus	34	= 2		
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RATE	FEE	OR		RATE	FEE	
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TOTAL		OR		TOTAL	1250	
<b>AMENDMENT B</b>						
(Column 1)		(Column 2)		(Column 3)		
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA			
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X39=		OR		X78=		
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TOTAL ADDITIONAL FEE		OR		TOTAL ADDITIONAL FEE		
<b>AMENDMENT C</b>						
(Column 1)		(Column 2)		(Column 3)		
AMENDMENT C	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA			
Total	0	Minus	0	= 0		
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+130=		OR		+260=		
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* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20." *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3." The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.						

 FORM PTO-575  
 (Rev. 6/98)  
 11/99

Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE

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SEARCHED			
Class	Sub.	Date	Exmr.
713	300	10-6-00	DMB
	320		
	322		
	500		
	501		
713	503	1-27-01	DMB
	300		
	326		
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	500		
	501		
	503		

INTERFERENCE SEARCHED			
Class	Sub.	Date	Exmr.
713	501	1-27-01	DMB
	503		
	300		

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	Date	Exmr.
STN Search (attached)	10-6-00	DMB
Internet Search	10-6-00	DMB
update Search	1-27-01	DMB

(RIGHT OUTSIDE)

FCS0000022

## ISSUE SLIP STAPLE AREA (for additional cross references)

POSITION	INITIALS	ID NO.	DATE
FEE DETERMINATION	D.B.	72203	11-28-98
O.L.P.E. CLASSIFIER		43	11-25-98
FORMALITY REVIEW		61581	12-12-98

## INDEX OF CLAIMS

✓ \_\_\_\_\_ Rejected      N \_\_\_\_\_ Non-elected  
 = \_\_\_\_\_ Allowed      I \_\_\_\_\_ Interference  
 - (Through numeral) \_\_\_\_\_ Canceled      A \_\_\_\_\_ Appeal  
 + \_\_\_\_\_ Restricted      O \_\_\_\_\_ Objected

Claim	Date	Claim	Date	Claim	Date
1	10/1	61		101	
2	10/27	62		102	
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If more than 150 claims or 10 actions  
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FCS0000023

MULTIPLE DEPENDENT CLAIM FEE CALCULATION SHEET (FOR USE WITH FORM PTO-426)							SERIAL NO. 09/192959 APPLICANT'S	FILING DATE					
CLAIMS													
	AS FILED		AFTER 1 <sup>st</sup> AMENDMENT		AFTER 2 <sup>nd</sup> AMENDMENT								
	IND.	DEF.	IND.	DEF.	IND.	DEF.		IND.	DEF.	IND.	DEF.	IND.	DEF.
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49							99						
50							100						
TOTAL IND.	16						TOTAL IND.						
TOTAL DEF.	29						TOTAL DEF.						

FCS0000024

**1**

**FCS0000025**

**APPLICATION  
FOR  
UNITED STATES LETTERS PATENT**

7/1/00  
00192959-111698

**TITLE: FREQUENCY-ITTING CONTROL**  
**APPLICANT: BALU BALAKRISHNAN, ALEX DJENGUERIAN, LEIF LUND**

"EXPRESS MAIL" Mailing Label Number EL1102151208

Date of Deposit Nov. 18, 1998

FCS0000026

PATENT  
ATTORNEY DOCKET NO: 10256/001001~~FREQUENCY-JITTERING-CORRECTOR~~Background

7/A

5 The present invention relates to an off-line switched mode control system with frequency jittering.

Many products rely on advanced electronic components to cost-effectively provide the product with the desired functionality. These electronic components require power regulation circuitry to supply them with a clean and steady source of power. The development of switched mode power supply technology has led to power supplies operating at high frequency to achieve small size and high efficiency. Each switched mode power supply typically relies on an oscillator switching at a fixed switching frequency or alternatively a variable frequency (such as in a ringing choke power supply).

Due to the high frequency operation relative to the frequency of an alternating current (AC) power line, switched mode power supplies can exacerbate problems associated with electromagnetic interference (EMI). EMI noise is generated when voltage and current are modulated by the switching power supply. This electrical noise can be transferred to the AC power line.

In addition to affecting the operation of other electronics within the vicinity of the power supply by conduction, EMI induced noise on a power line may radiate or leak from the power line and affect equipment which is not even connected to the power line. Both conducted and radiated electrical noise may adversely affect or interfere with the operation of the electronic equipment. For example, EMI noise generated by the switching power supply can cause problems for communication devices in the vicinity of the power supply. Radiated high frequency noise components may become a part of the AC mains signal and may be provided to other devices in the power grid. Further, power supply radiated EMI can interfere with radio and television transmissions.

35 To address EMI related interference, several specifications have been developed by government agencies in the United States

and in the European Community. These agencies have established specifications that define the maximum amount of EMI that can be produced by various classes of electronic devices. Since power  
 5 supplies generate a major component of the EMI for electronic devices, an important step in designing such supplies that conform to the specifications is to minimize EMI emission to the acceptable limits of the various specifications.

EMI may be reduced in a power supply by adding snubbers and  
 10 input filters. These components reduce the noise transferred to the power line and by so doing, also reduce the electric and magnetic fields of noise generated by the power line. While these methods can reduce EMI, they usually complicate the design process as well as increase the production cost. In practice, noise filtering components are added in an ad hoc manner and on a  
 15 trial-and-error basis during the final design process when EMI is found to exceed the compliance limits specified by the regulatory agencies. This inevitably adds unexpected costs to the products. Further, extra components can undesirably increase the size and weight of the power supply and thus the resulting product.

#### Summary of the Invention

EMI emission is reduced by jittering the switching frequency of a switched mode power supply. In one aspect, a frequency  
 20 jittering circuit varies the switching frequency using an oscillator for generating a switching frequency signal, the oscillator having a control input for varying the switching frequency. A digital to analog converter is connected to the control input for varying the switching frequency, and a counter  
 30 is connected to the output of the oscillator and to the digital to analog converter. The counter causes the digital to analog converter to adjust the control input and to vary the switching frequency.

Implementations of the invention include one or more of the  
 35 following. The oscillator has a primary current source connected to the oscillator control input. A differential switch may be

used with first and second transistors connected to the primary current source; a third transistor connected to the first transistor; and a fourth transistor connected to the second transistor at a junction. A capacitor and one or more comparators may be connected to the junction. The digital to analog converter has one or more current sources, with a transistor connected to each current source and to the counter. The primary current source may generate a current  $I$  and each of the current sources may generate a current lower than  $I$ . The current sources may generate binary weighted currents. The largest current source may generate a current which is less than about 0.1 of  $I$ .

In a second aspect, a method for generating a switching frequency in a power conversion system includes generating a primary current; cycling one or more secondary current sources to generate a secondary current which varies over time; and supplying the primary and secondary currents to a control input of an oscillator for generating a switching frequency which is varied over time.

Implementations of the invention include one or more of the following. A counter may be clocked with the output of the oscillator. The primary current may be generated by a current source. If the primary current is  $I$ , each of the secondary current sources may generate a supplemental current lower than  $I$  and which is passed to the oscillator control input. The supplemental current may be binary-weighted. The largest supplemental current may be less than approximately 0.1 of  $I$ .

In another aspect, a method for generating a switching frequency in a power conversion system includes generating a primary voltage; cycling one or more secondary voltage sources to generate a secondary voltage which varies over time; and supplying the primary and secondary voltages to a control input of a voltage-controlled oscillator for generating a switching frequency which is varied over time.



Implementations of the invention include one or more of the following. Where the primary voltage is  $V$ , each of the secondary voltage sources may generate a supplemental voltage lower than  $V$  which may be passed to the voltage-controlled oscillator. The supplemental voltage may be binary-weighted.

In another aspect, a frequency jittering circuit for varying a power supply switching frequency includes an oscillator for generating a switching frequency signal, the oscillator having a control input for varying the switching frequency; and means connected to the control input for varying the switching frequency.

Implementations of the invention include one or more of the following. The means for varying the frequency may include one or more current sources connected to the control input; and a counter connected to the output of the oscillator and to the one or more current sources. The oscillator may include a primary current source connected to the control input; and a differential switch connected to the primary current source. The differential switch may have first and second transistors connected to the primary current source; a third transistor connected to the first transistor; and a fourth transistor connected to the second transistor at a junction. A capacitor and a comparator may be connected to the junction. If the primary current source generates a current  $I$ , each of the current sources may generate a second current lower than the current  $I$ , further comprising a transistor connected to each current source connected to the counter. The means for varying the frequency may include one or more voltage sources connected to the control input; and a counter connected to the output of the oscillator and to the one or more voltage sources. The oscillator may include a primary voltage source connected to the control input; and a differential switch connected to the primary voltage source. The means for varying the frequency may include a capacitor; a current source adapted to charge the capacitor; and means for alternately charging and discharging the capacitor. One or more comparators

may be connected to the capacitor and the means for alternately charging and discharging the capacitor.

In yet another aspect, a power supply includes a transformer, an oscillator for generating a signal having a frequency, the oscillator having a control input for varying the frequency of the signal, the oscillator including a primary current source connected to the control input; a differential switch connected to the primary current source; a capacitor connected to the differential switch; and a comparator connected to the differential switch. The power supply also includes a digital to analog converter connected to the control input, the analog to digital converter having one or more current sources, wherein the primary current source generates a current  $I$  and each of the current sources generates a current lower than  $I$ . A counter is connected to the output of the oscillator and to the current sources of the digital to analog converter. Further, a power transistor is connected to the primary winding of the transformer so that when the power transistor is modulated, a regulated power supply output is provided.

In another aspect, a power supply includes a transformer connected to an input voltage. The power supply includes an oscillator for generating a signal having a frequency, the oscillator having a control input for varying the frequency of the signal, the oscillator including: a primary current source connected to the control input; a differential switch connected to the primary current source; a capacitor connected to the differential switch; and a comparator connected to the differential switch. A circuit for varying the frequency is connected to the control input, the circuit having a capacitor; a current source adapted to charge and discharge the capacitor; one or more comparators connected to the capacitor to the current source for alternately charging and discharging the capacitor. Further, a power transistor is connected to the oscillator and to the primary winding. The power transistor modulates its output in providing a regulated power supply output.

Advantages of the invention include one or more of the following. The jittering operation smears the switching frequency of the power supply over a wide frequency range and thus spreads energy outside of the bandwidth measured by the EMI measurement equipment. By changing the oscillator frequency back and forth, the average noise measured by the EMI measurement equipment is reduced considerably.

Further, the invention provides the required jittering without requiring a large area on the regulator chip to implement a capacitor in a low frequency oscillator. Further, the invention minimizes effects caused by leakage current from transistors and capacitors associated with a low frequency oscillator. Thus, the jittering operation can be maintained even at high temperature which can increase current leakage.

Additionally, the invention reduces the need to add extra noise filtering components associated with the EMI filter. Therefore a compact and inexpensive power supply system can be built with minimal EMI emissions.

#### Brief Description of the Drawings

Fig. 1 is a schematic diagram of a digital frequency jittering device.

Fig. 2 is a plot illustrating the operation of the device of Fig. 1.

Fig. 3 is a schematic diagram of an analog frequency jittering device.

Fig. 4 is a schematic diagram of an implementation of the device of Fig. 3.

Fig. 5 is a timing diagram illustrating the operation of the frequency jitter device of Fig. 4.

Fig. 6 is a schematic diagram of a switched mode power supply in accordance with the present invention.

#### Description

Fig. 1 shows a digital frequency jittering circuit 100. The digital frequency jittering circuit 100 has a primary oscillator 110 which provides a clock signal to a counter 140. The primary oscillator 110 typically operates between 100 kHz and 130 kHz. The counter 140 can be a seven bit counter. Each output of counter 140, when clocked by primary oscillator 110, represents a particular time interval. The outputs of the counter 140 are provided to a series of frequency jittering current sources 150. The outputs of the series of frequency jittering current sources 150 are presented to the primary oscillator 110 to vary its frequency, as will be described below.

Primary oscillator 110 contains a primary current source 122 which provides a primary current (denoted as I) to node 123. Current 125 to the node 123 is provided to the source of MOSFET transistors 126 and 132. The drain of MOSFET transistor 126 is connected to the drain of an n-channel MOSFET transistor 128. The source of transistor 128 is grounded, while the gate of the transistor 128 is connected to its drain. The gate of the transistor 128 is also connected to the gate of an n-channel MOSFET transistor 130. The source of the transistor 130 is grounded while the drain is connected to the drain of the MOSFET transistor 132 at a node 131. Transistors 126, 128, 130 and 132 form a differential switch. The output of comparator 136 is connected to the gate of the transistor 132 and to an inverter 124. The output of inverter 124 is connected to the gate of transistor 126. The comparator 136 has an input which is connected to node 131 and to a capacitor 134. In combination, the transistors 126, 128, 130 and 132, capacitor 134, inverter 124, current source 122 and comparator 136 form an oscillator. The output of the comparator 136 is provided as an oscillator output OSC\_OUT 101 and is also used to drive the clock input of counter 140.

Counter 140 has a plurality of outputs Q1-Q3 (not shown) which are not used. The remaining outputs Q4-Q7 are connected to

a digital-to-analog (D-to-A) converter 150, which may be  
 implemented as a series of frequency jittering voltage sources or  
 current sources. A Q4 output 155 is connected to the gate of a  
 5 p-channel MOSFET transistor 154. A Q5 output 157 is connected to  
 the gate of a p-channel MOSFET transistor 158. The Q6 output 163  
 is connected to the gate of a p-channel MOSFET transistor 162,  
 and Q7 output 167 is connected to the gate of a p-channel MOSFET  
 transistor 166. When D-to-A converter 150 is viewed as a  
 10 plurality of current sources, the source of transistor 154 is  
 connected to a jittering current source 152, which provides a  
 current which is  $1/200$ th of the current I generated by the  
 current source 122. The source of MOSFET transistor 158 is  
 connected to a current source 156 which provides a current that  
 15 is  $1/100$ th of the current I. The source of the MOSFET transistor  
 162 is connected to a jittering current source 160 which provides  
 a current that is  $1/50$ th of I. Finally, the source of the MOSFET  
 transistor 166 is connected to a jittering current source 164  
 which provides a current that is  $1/25$ th of the current I. The  
 current sources 152, 156, 160 and 164 are binary-weighted, that  
 is, the current source 164 provides twice the current provided by  
 the current source 160, the current source 160 provides twice the  
 current supplied by the current source 156 and the current source  
 156 provides twice the current provided by the current source  
 152.

Further, in one embodiment, the largest current source 164  
 may supply no more than 10% of the current I provided by the  
 primary current source 122. The drain of transistors 154, 158,  
 162 and 166 are joined together such that the supplemental  
 30 frequency jittering current sources of the D-to-A converter 150  
 can be provided to supplement the primary current source 122.

During operation, at every eight clock cycles, the counter  
 output Q4 on line 155 changes state. Similarly, at every 16  
 clock cycles, the output Q5 on line 157 changes state and at  
 35 every 32 clock cycles, the output Q6 on line 163 changes state,  
 and every 64 clock cycles, the output Q7 on line 167 changes

state. The entire counting cycle thereafter repeats itself. Each time the output Q4 on line 155 is low, transistor 154 is turned on to inject current in the amount of  $I/200$  to node 123 so that the total current 125 is  $1.005I$ . Similarly, each time that the output Q5 on line 157 is low, transistor 158 is turned on to inject current in the amount of  $I/100$  to node 123 so that the total current 125 is  $1.01I$ . Further, each time that output Q6 on line 163 is low, transistor 162 is turned on to inject current in the amount of  $I/50$  to node 123 so that the total current 125 is  $1.02I$ . Finally, each time that the output Q7 on line 167 is low, the transistor 166 is turned on to inject current in the amount of  $I/25$  to node 123 so that the total current 125 is  $1.04I$ .

Additionally, when combinations of outputs Q4-Q7 are turned on, the outputs of the respective current sources 152, 156, 160 and 164 are added to the output of current source 122 to vary the frequency of the primary oscillator 110. In this manner, counter 140 drives a plurality of current sources to inject additional current to the main current source 122 such that the frequency of the primary oscillator 110 is varied.

The jittering operation of the embodiment of Figure 1 is further illustrated in a chart in Figure 2. A normalized operating frequency is plotted on the y-axis while the counting cycle as shown by the counter outputs Q4-Q7 is plotted on the x-axis. As shown in Figure 2, as the counter counts upward to the maximum count of 128, the peak switching frequency is achieved. This peak switching frequency is normalized to be about 1.075 times the base switching frequency. Further, on average, the switching frequency is between 1.03 and 1.04 times the base switching frequency. Thus, the embodiment of Figure 1 deviates the switching frequency of the oscillator within a narrow range. This deviation reduces EMI noise by spreading the energy over a wider frequency range than the bandwidth measured by the EMI test equipment such that the noise measured by the EMI test equipment is reduced considerably.

Figure 3 shows an analog frequency jittering circuit. More details on the analog frequency jittering device are shown in co-  
 pending U.S. Application Serial No. 09/080,774, entitled "OFFLINE  
 5 CONVERTER WITH INTEGRATED SOFT START AND FREQUENCY JITTER," filed  
 on May 18, 1998, the content of which is hereby incorporated by  
 reference. In Fig. 3, the primary oscillator 110 provides an  
 oscillator output on line OSC-OUT 101. An analog low frequency  
 oscillator 405 is also provided. Primary oscillator 110  
 10 typically operates between a range of 30 to 300 kHz, while the  
 low frequency oscillator 405 typically operates between a range  
 of 5 Hz to 5 kHz. As discussed above, the switching frequency of  
 the primary oscillator 110 is determined by the amount of current  
 the primary oscillator uses to charge and discharge capacitor  
 134. The low frequency oscillator 405 varies this current within  
 15 a narrow range to jitter the frequency of the primary oscillator  
 110.

The output of low frequency oscillator 405 is provided to a  
 MOSFET transistor 505 connected to a resistor 510 and a current  
 mirror including transistors 495 and 500. Transistor 500 is  
 connected to node 123 so that extra current can be added to  
 current source 122 feeding the primary oscillator. In this  
 manner, the frequency of the primary oscillator 110 is shifted  
 around a narrow range to reduce the EMI noise.

Figure 4 shows a more detailed implementation of Figure 3.  
 As shown therein, main oscillator 465 has a current source 470  
 that is mirrored by current mirror transistors 472 and 475. Main  
 oscillator drive current 615 is provided to current source input  
 485 of oscillator 480. The magnitude of the current input into  
 30 current source input 485 determines the frequency of the  
 oscillation signal 415 provided by oscillator 480. In order to  
 vary the frequency of the oscillation signal 415, an additional  
 current source 495 is provided within the main oscillator 465.  
 The current source 495 is mirrored by current source mirror 500.

35 The current provided by current source 495 is varied as  
 follows. Frequency variation signal 400 is provided to the gate

of main oscillator transistor 505. As the magnitude of frequency variation signal 400 increases, so does the voltage at the source of main oscillator transistor 505 due to the increasing voltage at the gate of the transistor 505 and the relatively constant voltage drop between the gate and source of the transistor 505. As the voltage at the source of transistor 505 increases, so does the current 604 flowing through the resistor 510. The current flowing through the resistor 510 is the same as the current flowing through additional current source 500 which mirrors transistor 495.

Since the frequency variation signal 400 is a triangular waveform having a fixed period, as shown, the magnitude of the current input by additional current source mirror 500 will vary linearly with the magnitude of the rising and falling edges of the frequency variation signal 400. If the frequency variation signal 400 is a ramp signal, the frequency will linearly rise to a peak and then fall to its lowest value. In this way, the current 615 provided to current source input 485 of the oscillator 480 is varied in a known fixed range that allows for an easy and accurate frequency spread of the high frequency current. Further, the variance of the frequency is determined by the magnitude of the current provided by current source mirror 500, which is a function of the resistance of the resistor 510.

Frequency variation circuit 405 includes a current source 525 that produces a fixed magnitude current 530 that determines the magnitude of the frequency of the frequency variation signal 400. Although the current 530 has a fixed magnitude, the frequency variation signal can be generated utilizing a variable magnitude current. If such variable current is generated, the frequency spread is not fixed in time but varies with the magnitude of current 530. The fixed magnitude current 530 is fed into first transistor 535, mirrored by second transistor 540 and third transistor 545. The frequency variation signal 400 is generated by the charging and discharging of the capacitor 550. Frequency variation circuit capacitor 550 has a relatively low



capacitance, which allows for integration into a monolithic chip in one embodiment of low frequency oscillator 405. The frequency variation signal 400 is provided to upper limit comparator 555 and lower limit comparator 560. The output of upper limit comparator 555 will be high when the magnitude of the frequency variation signal 400 exceeds the upper threshold voltage on line 552 which is about 4.5 volts. The output of lower limit comparator 560 will be low when the magnitude of frequency variation signal 400 drops below lower threshold voltage on line 557 which is about 1.5 volts. The output of upper limit comparator 555 is provided to the frequency variation circuit inverter 565 the output of which is provided to the reset input of frequency variation circuit latch 570. The set input of frequency variation circuit latch 570 receives the output of lower limit comparator 560.

In operation, the output of lower limit comparator 560 will be maintained high for the majority of each cycle of frequency variation signal 400 because the magnitude of frequency variation signal will be maintained between the upper threshold on line 552, 4.5 volts, and lower threshold on line 557, 1.5 volts. The output of upper limit comparator 555 will be low until the magnitude of frequency variation signal 400 exceeds upper level threshold on line 552. This means that the reset input will receive a high signal when the magnitude of the frequency variation signal 400 rises above the upper threshold signal on line 552.

The charge signal 575 output by frequency variation circuit latch 570 will be high until the frequency variation signal 400 exceeds the upper threshold limit signal on line 552. When the charge signal 575 is high, transistors 585 and 595 are turned off. By turning off transistors 585 and 595, current can flow into the capacitor 550, which steadily charges capacitor 550 and increases the magnitude of frequency variation signal 400. The current that flows into the capacitor 550 is derived from current source 525 because the current through transistor 590 is mirrored

from transistor 580, which in turn is mirrored from transistor 535.

During power up, when power-up signal 420 is low, the output of inverter 605 is high, which turns on transistor 600, causing frequency variation signal 400 to go low. The frequency variation signal 400 starts from its lowest level to perform a soft start function during its first cycle of operation.

Referring to Figs. 4 and 5, Fig. 5 shows the operation of the analog frequency jittering device of Figure 4. In Figure 5, a frequency variation signal 405 is provided to the main oscillator 465. The magnitude of the current 615 is approximately the magnitude of the frequency variation signal 405, less the threshold voltage of transistor 505, and divided by the resistance of the resistor 510 plus the magnitude of the current produced by the current source 475. The current 615 varies with the magnitude of the frequency variation signal 405. The variation of the current 615 in turn varies the frequency of the oscillator clock.

Referring now to Figure 6, a switched mode power supply is shown. Direct current (DC) input voltage is provided to a Zener diode 912 which is connected to a diode 914. The diodes 912-914 together are connected in series across a primary winding of a transformer 920. A secondary winding 922 is magnetically coupled to the primary winding of transformer 920. One terminal of the secondary winding 922 is connected to a diode 930, whose output is provided to a capacitor 932. The junction between diode 930 and capacitor 932 is the positive terminal of the regulated output. The other terminal of capacitor 932 is connected to a second terminal of the secondary winding and is the negative terminal of the regulated output. A Zener diode 934 is connected to the positive terminal of the regulated output. The other end of Zener diode 934 is connected to a first end of a light emitting diode in an opto-isolator 944. A second end of the light-emitting diode is connected to the negative terminal of the regulated output. A resistor 936 is connected between the

negative terminal of the regulated output and the first end of the light-emitting diode of opto-isolator 944. The collector of the opto-isolator 944 is connected to current source 172. The output of current source 172 is provided to the switching regulator logic 800.

Connected to the second primary winding terminal is the power transistor 208. Power transistor 208 is driven by the switching regulator logic 800. Switching regulator logic 800 receives a clock signal 101 from an oscillator 111. A counter 140 also receives the clock signal 101 from the primary oscillator 111. The outputs of counter 140 are provided to D-to-A converter 150, which is connected to oscillator 111 for jittering the oscillation frequency. Alternatively, in lieu of counter 140 and a D-to-A converter 150, an analog low frequency jittering oscillator may be used.

The foregoing disclosure and description of the invention are illustrative and explanatory thereof, and various changes in the size, shape, materials, components, circuit elements, wiring connections and contacts, as well as in the details of the illustrated circuitry and construction and method of operation may be made without departing from the spirit of the invention.

What is claimed is:

- 1 1. A digital frequency jittering circuit for varying the  
2 switching frequency of a power supply, comprising:  
3 an oscillator for generating a signal having a switching  
4 frequency, the oscillator having a control input for varying the  
5 switching frequency;  
6 a digital to analog converter coupled to the control input  
7 for varying the switching frequency; and  
8 a counter coupled to the output of the oscillator and to the  
9 digital to analog converter, the counter causing the digital to  
10 analog converter to adjust the control input and to vary the  
11 switching frequency.
- 1 2. The circuit of claim 1, wherein the oscillator further  
2 comprises a primary current source coupled to the oscillator  
3 control input.
- 1 3. The circuit of claim 2, further comprising a differential  
2 switch, including:  
3 first and second transistors coupled to the primary current  
4 source;  
5 a third transistor coupled to the first transistor; and  
6 a fourth transistor coupled to the second transistor at a  
7 junction.
- 1 4. The circuit of claim 3, further comprising a capacitor  
2 coupled to the junction.
- 1 5. The circuit of claim 3, further comprising one or more  
2 comparators coupled to the junction.
- 1 6. The circuit of claim 2, wherein the digital to analog  
2 converter has one or more secondary current sources.
- 1 7. The circuit of claim 6, further comprising a transistor  
2 coupled between each secondary current source and the counter.

1 8. The circuit of claim 6, wherein the primary current source  
2 generates a current  $I$  and each of the secondary current sources  
3 generates a current lower than  $I$ .

1 9. The circuit of claim 8, wherein the secondary current  
2 sources generate binary weighted currents.

1 10. The circuit of claim 8, wherein the largest secondary  
2 current source generates a current which is less than about 0.1  
3 of  $I$ .

5.6  
1 11. A method for generating a switching frequency in a power  
2 conversion system, comprising:  
generating a primary current;  
cycling one or more secondary current sources to generate a  
secondary current which varies over time; and  
supplying the primary and secondary currents to a control  
input of an oscillator for generating a switching frequency which  
is varied over time.

12. The method of claim 11 further comprising the step of  
clocking a counter with the output of the oscillator.

13. The method of claim 11 wherein the primary current is  
2 generated by a current source.

1 14. The method of claim 11 wherein the primary current is  $I$  and  
2 each of the secondary current sources generates a supplemental  
3 current lower than  $I$ , and further comprising passing the  
4 supplemental current to the oscillator control input.

1 15. The method of claim 14 further comprising binary-weighting  
2 the supplemental current.

1 16. The method of claim 14 wherein the largest supplemental  
2 current is less than approximately 0.1 of I.

Sub  
Q31  
17. A method for generating a switching frequency in a power  
conversion system, comprising:  
3 generating a primary voltage;  
4 cycling one or more secondary voltage sources to generate a  
5 secondary voltage which varies over time; and  
6 supplying the primary and secondary voltages to a control  
7 input of a voltage-controlled oscillator for generating a  
8 switching frequency which is varied over time.

1 18. The method of claim 17 further comprising clocking a counter  
2 with the output of the oscillator.

19. The method of claim 17 wherein the primary voltage is V and  
each of the secondary voltage sources generates a supplemental  
voltage lower than V, further comprising passing the supplemental  
voltage to the voltage-controlled oscillator.

20. The method of claim 19, wherein the supplemental voltage is  
binary-weighted.

Sub  
Q32  
21. A frequency jittering circuit for varying a power supply  
switching frequency, comprising:  
3 an oscillator for generating a signal having a switching  
4 frequency, the oscillator having a control input for varying the  
5 switching frequency; and  
6 means coupled to the control input for varying the switching  
7 frequency.

1 22. The circuit of claim 21 wherein the means for varying the  
2 frequency further comprises:  
3 one or more current sources coupled to the control input;  
4 and-

5 a counter coupled to the output of the oscillator and to the  
6 one or more current sources. *10a*

1 23. The circuit of claim 22 wherein the oscillator further  
2 comprises:  
3 a primary current source coupled to the control input; and  
4 a differential switch coupled to the primary current source.

1 24. The circuit of claim <sup>22</sup>23 wherein the differential switch  
2 further comprises:  
3 first and second transistors coupled to the primary current  
4 source;  
5 a third transistor coupled to the first transistor; and  
6 a fourth transistor coupled to the second transistor at a  
junction.

1 25. The circuit of claim <sup>22</sup>24 further comprising a capacitor and a  
2 comparator coupled to the junction.

1 26. The circuit of claim 22 further comprising a transistor  
2 coupled to each current source and to the counter.

1 27. The circuit of claim 22 wherein the primary current source  
2 generates a current I and each of the current sources generates a  
3 current lower than I.

1 28. The circuit of claim 22 wherein the primary current source  
2 generates a current I and each of the current sources generates a  
3 second current lower than the current I, further comprising a  
4 transistor coupled to each current source connected to the  
5 counter.

1 29. The circuit of claim 21 wherein the means for varying the  
2 frequency further comprises: *10a*

3 one or more voltage sources coupled to the control input;  
 4 and  
 5 a counter coupled to the output of the oscillator and to the  
 6 one or more voltage sources.

Sub  
A2  
30. The circuit of claim 22 wherein the oscillator further  
 comprises:  
 3 a primary voltage source coupled to the control input; and  
 4 a differential switch coupled to the primary voltage source.

29  
 1 The circuit of claim 21 wherein the means for varying the  
 2 frequency further comprises:  
 3 a capacitor; and  
 4 a current source adapted to charge and discharge the  
 capacitor.

Sub  
A7  
 32. The circuit of claim 31 further comprising:  
 one or more comparators coupled to the capacitor; and  
 the means for alternately charging and discharging the  
 capacitor.

33. A power supply having a transformer coupled to an input  
 voltage, the transformer having a primary winding, the power  
 supply comprising:  
 an oscillator for generating a signal having a frequency,  
 5 the oscillator having a control input for varying the frequency  
 6 of the signal, the oscillator including:  
 7 a primary current source coupled to the control input;  
 8 a differential switch coupled to the primary current  
 9 source;  
 10 a capacitor coupled to the differential switch; and  
 11 a comparator coupled to the differential switch;  
 12 a digital to analog converter coupled to the control input,  
 13 the analog to digital converter having one or more current



14 sources, wherein the primary current source generates a current  $I$   
 15 and each of the current sources generates a current lower than  $I$ ;  
 16 a counter coupled to the output of the oscillator and to the  
 17 current sources of the digital to analog converter; and  
 18 a power transistor coupled to the oscillator and to one  
 19 terminal of the primary winding, the power transistor modulating  
 20 its output in providing a regulated power supply output.

1 34. A power supply having a transformer coupled to an input  
 2 voltage, the transformer having a primary winding, the power  
 3 supply comprising:  
 4 an oscillator for generating a signal having a frequency,  
 5 the oscillator having a control input for varying the frequency  
 6 of the signal, the oscillator including:  
 . a primary current source coupled to the control input;  
 a differential switch coupled to the primary current  
 source;  
 a capacitor coupled to the differential switch; and  
 a comparator coupled to the differential switch;  
 a circuit for varying the frequency, the circuit coupled to  
 the control input, including:  
 a capacitor;  
 a current source adapted to charge and discharge the  
 capacitor;  
 one or more comparators coupled to the capacitor to the  
 18 current source for alternately charging and discharging the  
 19 capacitor; and  
 20 a power transistor coupled to the oscillator and to one  
 21 terminal of the primary winding, the power transistor modulating  
 22 its output in providing a regulated power supply output.

09/192959

Abstract

EMI emission is reduced by jittering the switching frequency of a switched mode power supply. An oscillator with a control input for varying the oscillator's switching frequency generates a jittered clock signal. In one embodiment, the oscillator is connected to a counter clocked by the oscillator. The counter drives a digital to analog converter, whose output is connected to the control input of the oscillator for varying the oscillation frequency. In another embodiment, the oscillator is connected to a low frequency oscillator whose low frequency output is used to supplement the output of the oscillator for jittering the switching frequency. The invention thus deviates or jitters the switching frequency of the switched mode power supply oscillator within a narrow range to reduce EMI noise by spreading the energy over a wider frequency range than the bandwidth measured by the EMI test equipment.

PCLSO.MAL

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09/192959

PATENT  
ATTORNEY'S DOCKET NO: 10256/003601

## COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled FREQUENCY JITTERING CONTROL, the specification of which is attached hereto.

☐ was filed on \_\_\_\_\_ as Application Serial No. \_\_\_\_\_  
and was amended on \_\_\_\_\_  
☐ was described and claimed in PCT International Application No. \_\_\_\_\_  
filed on \_\_\_\_\_ and as amended under  
PCT Article 19 on \_\_\_\_\_.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose all information I know to be material to patentability in accordance with Title 37, Code of Federal Regulations, §1.56.

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose all information I know to be material to patentability as defined in Title 37, Code of Federal Regulations, §1.56(a) which became available between the filing date of the prior application and the national or PCT international filing date of this application:

I hereby appoint the following attorneys and/or agents to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith: Roger S. Borovoy, Reg. No. 20,193, Hans R. Troesch, Reg. No. 36,950, William J. Egan, III, Reg. No. 48,511, Bao Q. Tran, Reg. No. 37,933, David J. Goren, Reg. No. 34,609, Mark D. Kirkland, Reg. No. 40,048, Wayne P. Sobon, Reg. No. 32,438, Christopher P. Rogers, Reg. No. 36,334, Edouard A. Garcia, Reg. No. 38,461,

Address all telephone calls to Bao Q. Tran at telephone number 650/322-5070.

Address all correspondence to Roger S. Borovoy, Fish & Richardson P.C., 2200 Sand Hill Road, Suite 100, Menlo Park, CA 94025.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patents issued thereon.

Full Name of Inventor: Bala Balakrishnan

Inventor's Signature: Bala Balakrishnan Date: 11-13-1998

Residence Address: Saratoga, California

Citizen of: U.S.A.

Post Office Address: 13917 Altair Court, Saratoga, CA 95070

Revised August 24 1994 (39)DBCL(MRG)

09192959-111608

FCS0000048

COMBINED DECLARATION AND POWER OF ATTORNEY CONTINUED

Full Name of Inventor: Alex Djengue

Inventor's Signature: Alex Djengue Date: Nov. 13, 1998

Residence Address: Saratoga, California

Citizen of: U.S.A.

Post Office Address: 20602 Sevilla Lane, Saratoga, CA 95070

Full Name of Inventor: Leif Lund

Inventor's Signature: Leif Lund Date: Nov. 13, 1998

Residence Address: San Jose, California

Citizen of: Sweden

Post Office Address: 1074 Quincebrook Drive, San Jose, CA 95129

WITNESSES

Revised: August 24 1994 (9108CLJ&L)

FCS0000049

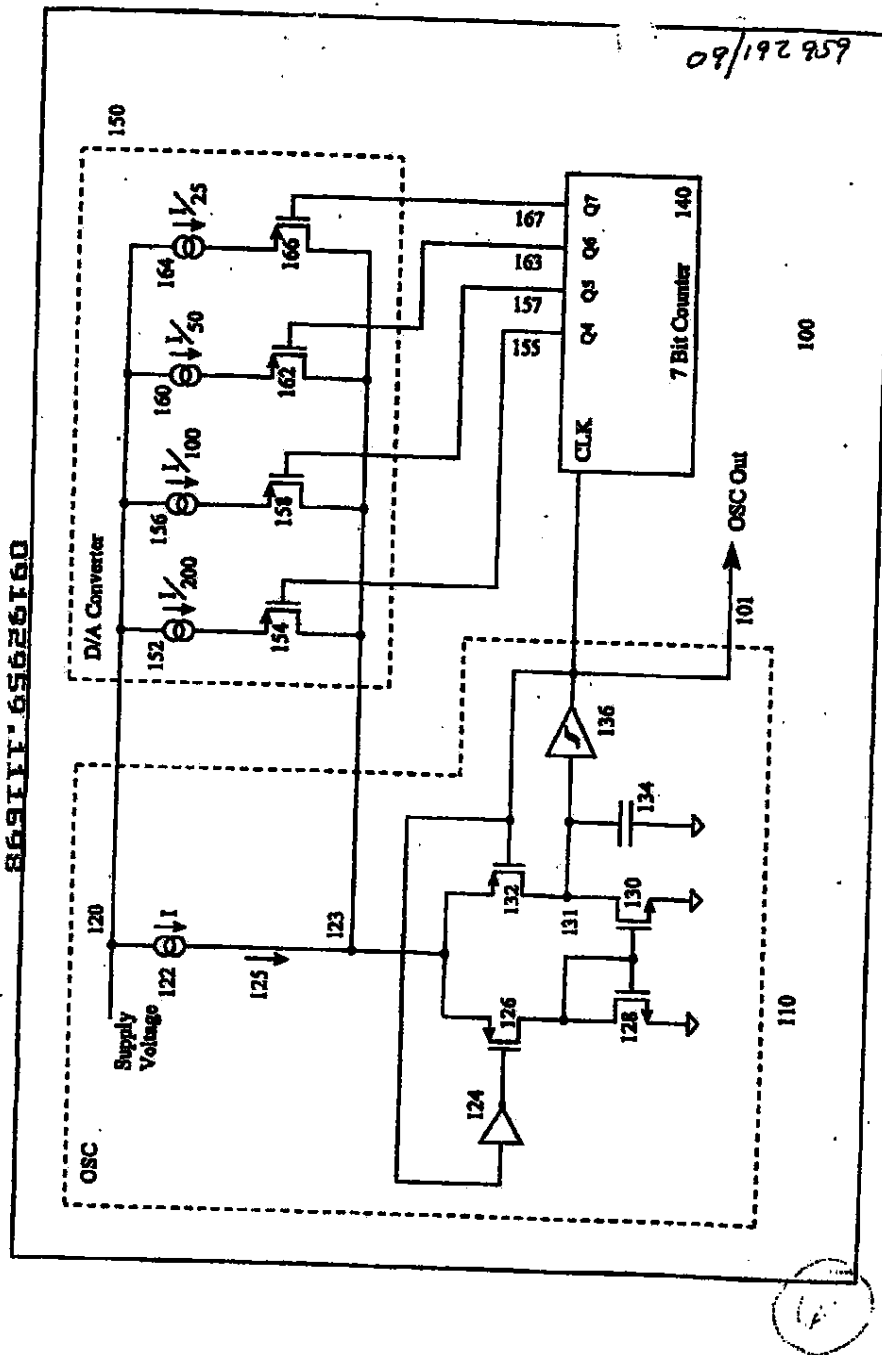


Figure 1.

869111-65626160

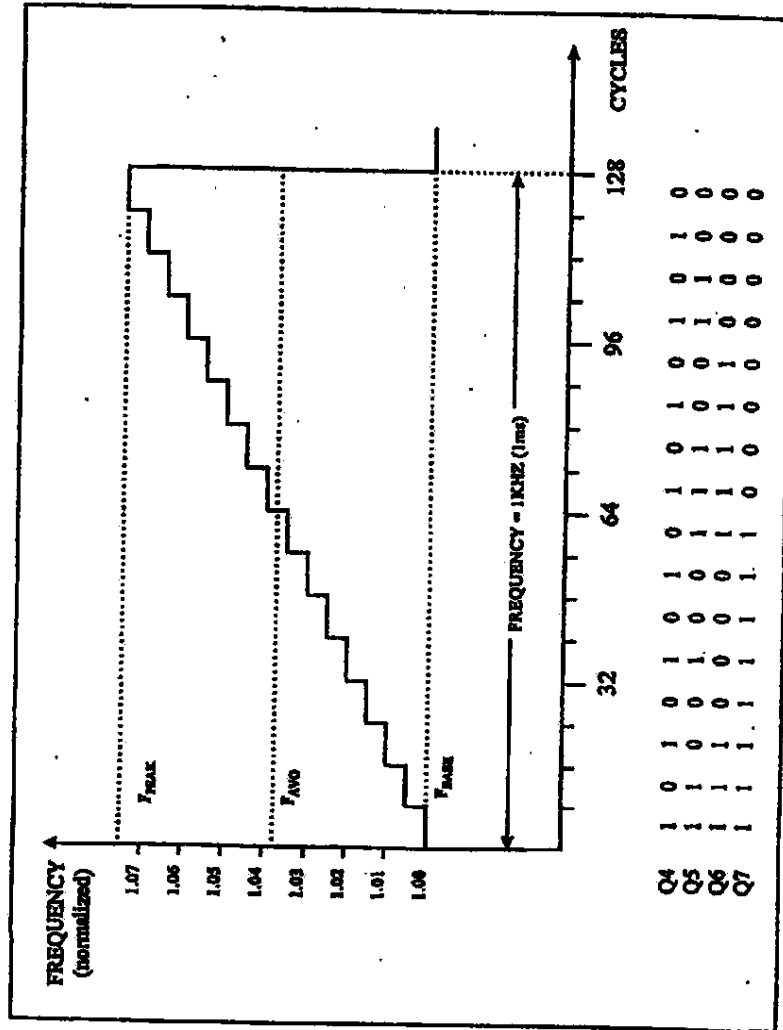


Figure 2.

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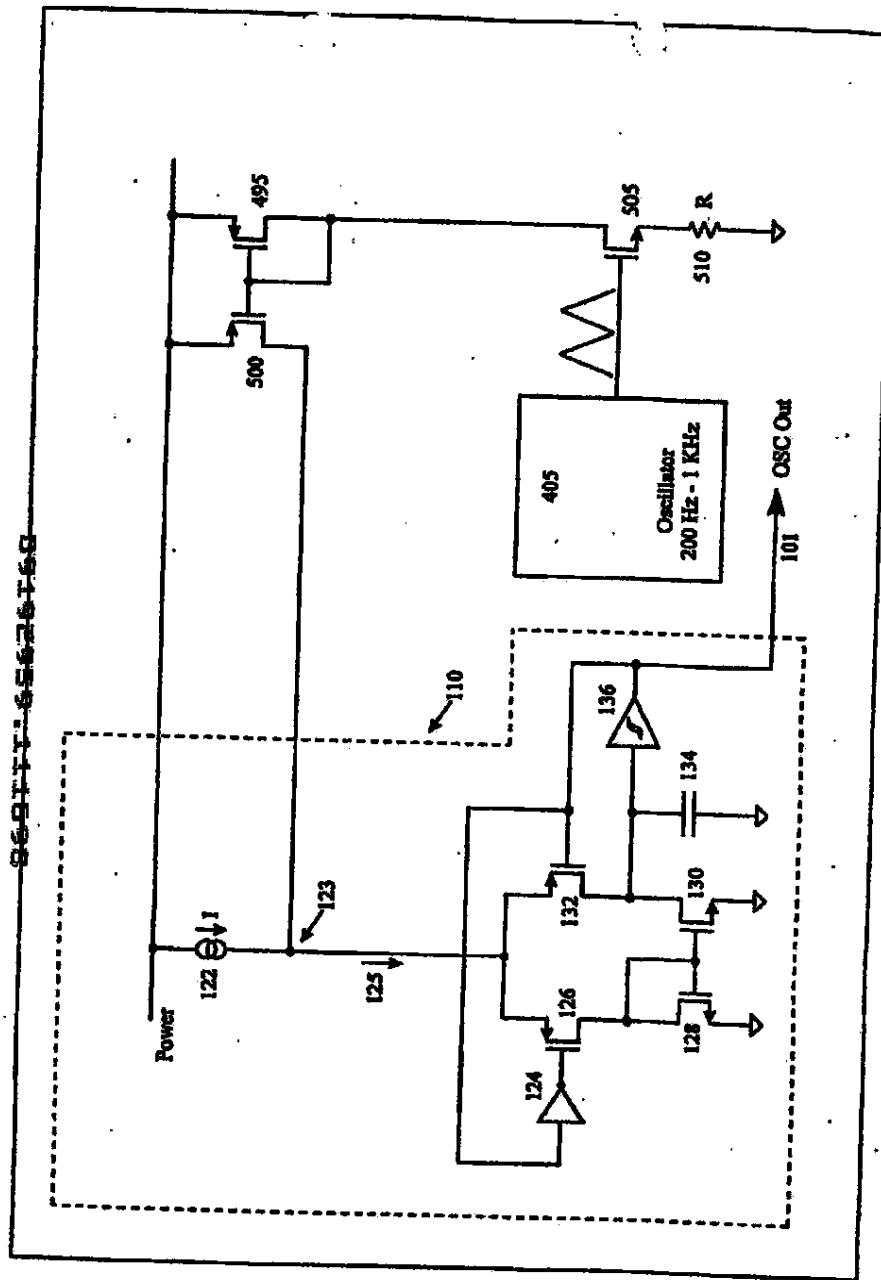


Figure 3.

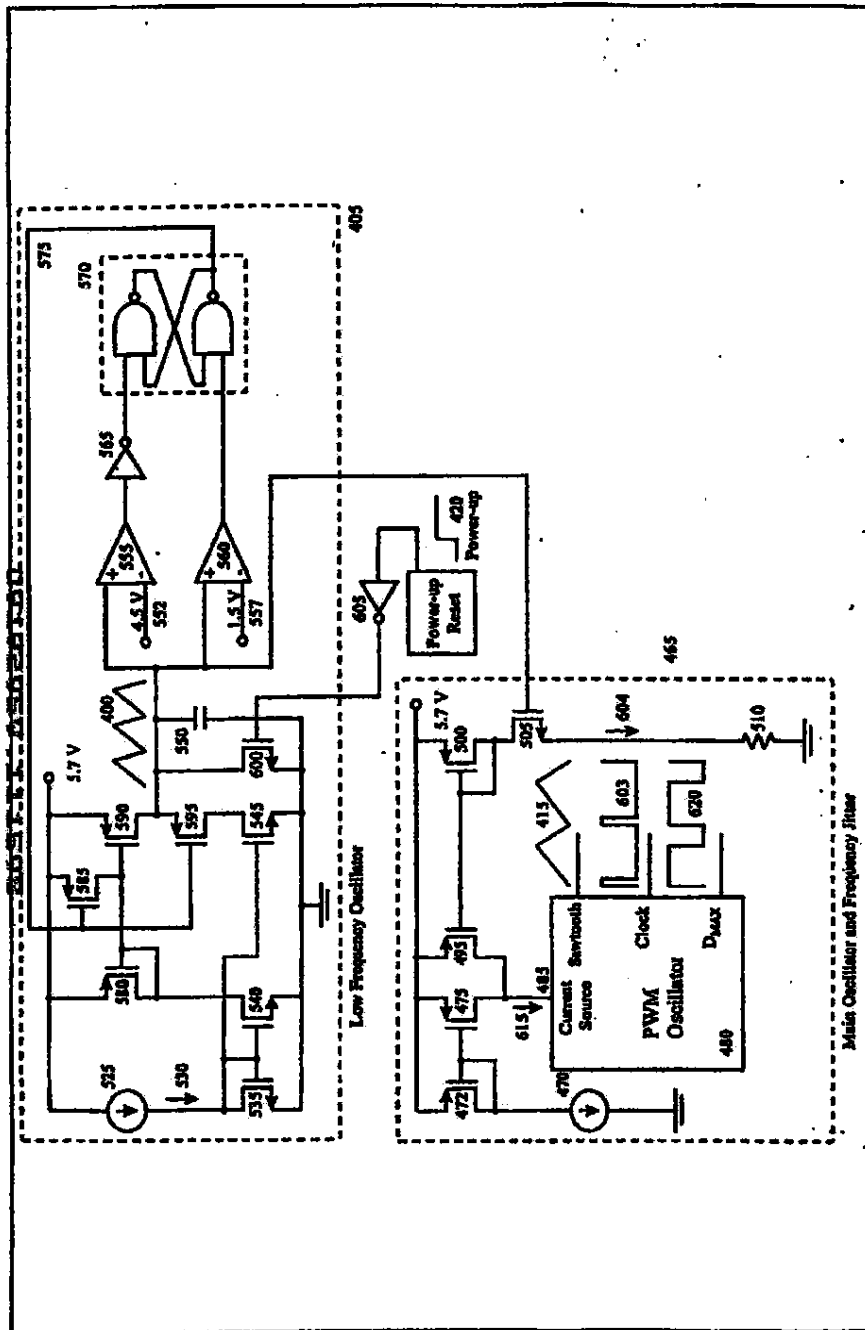


Figure 4.



869TT-65626T60

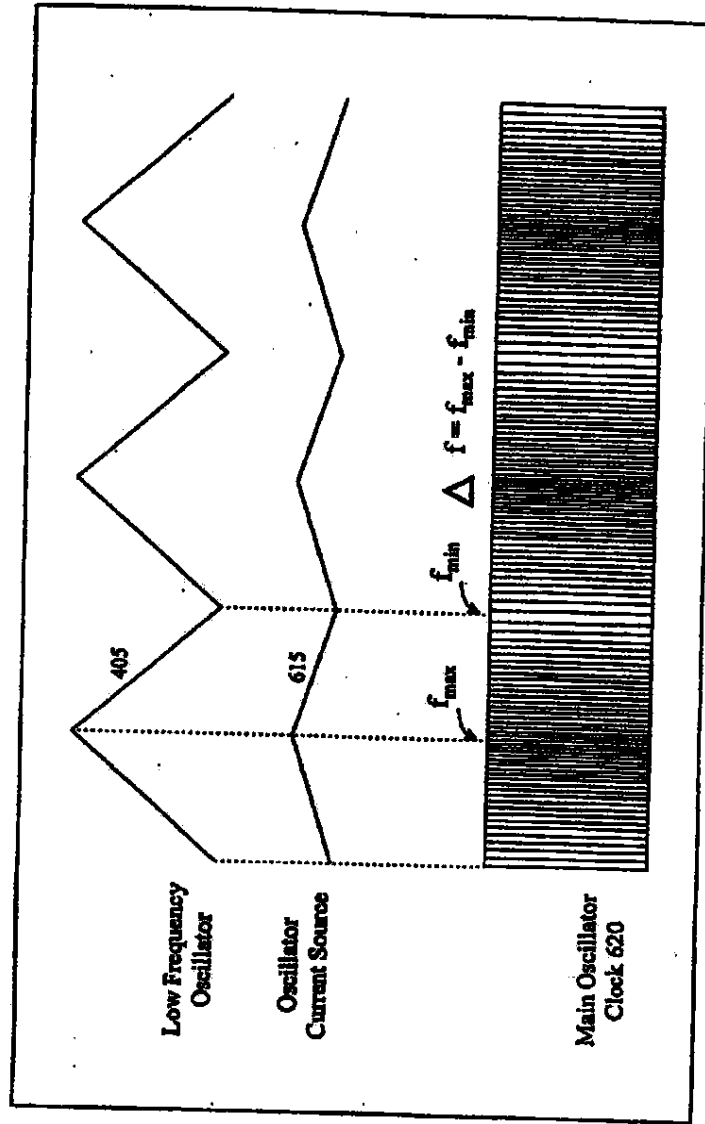
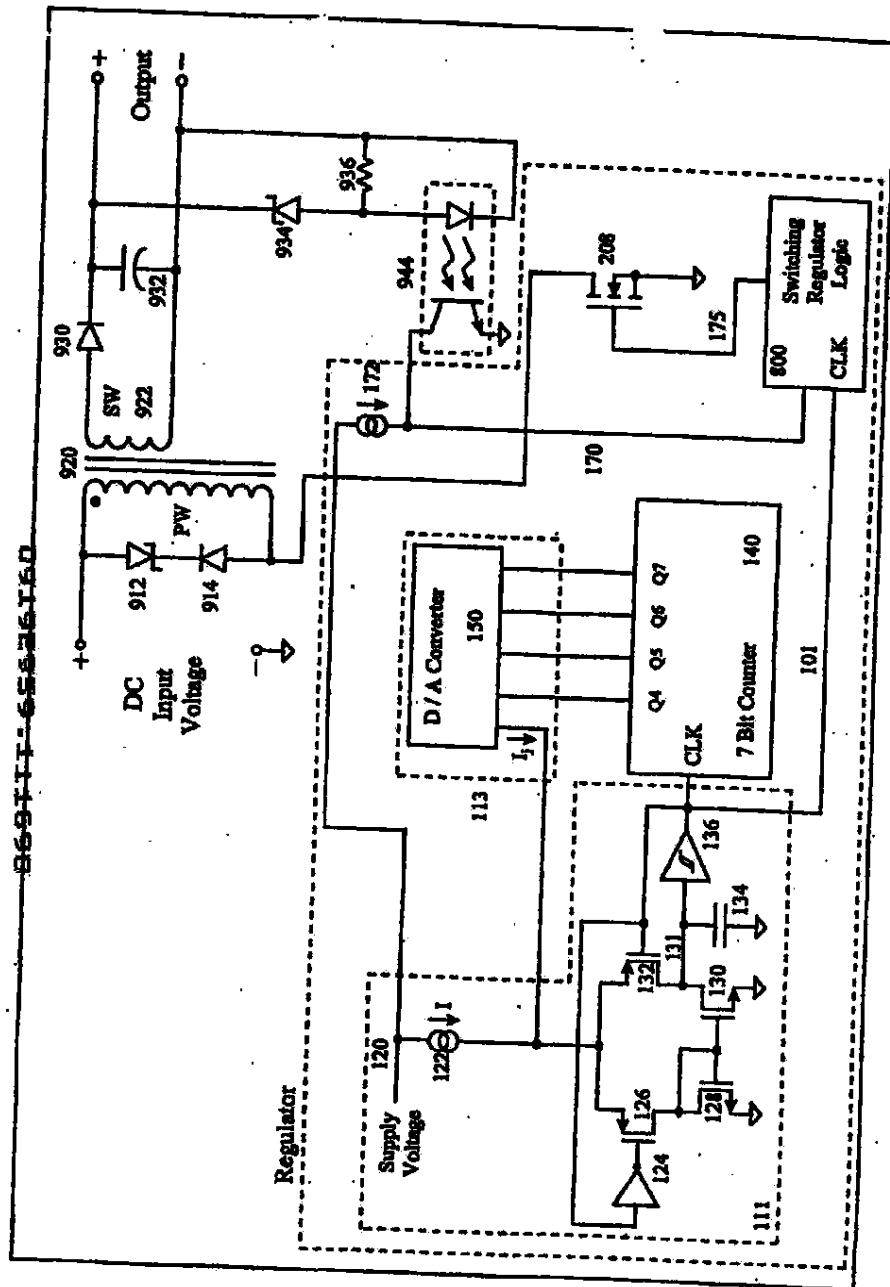


Figure 5.



**पुनर्विचार**

**FCS0000055**

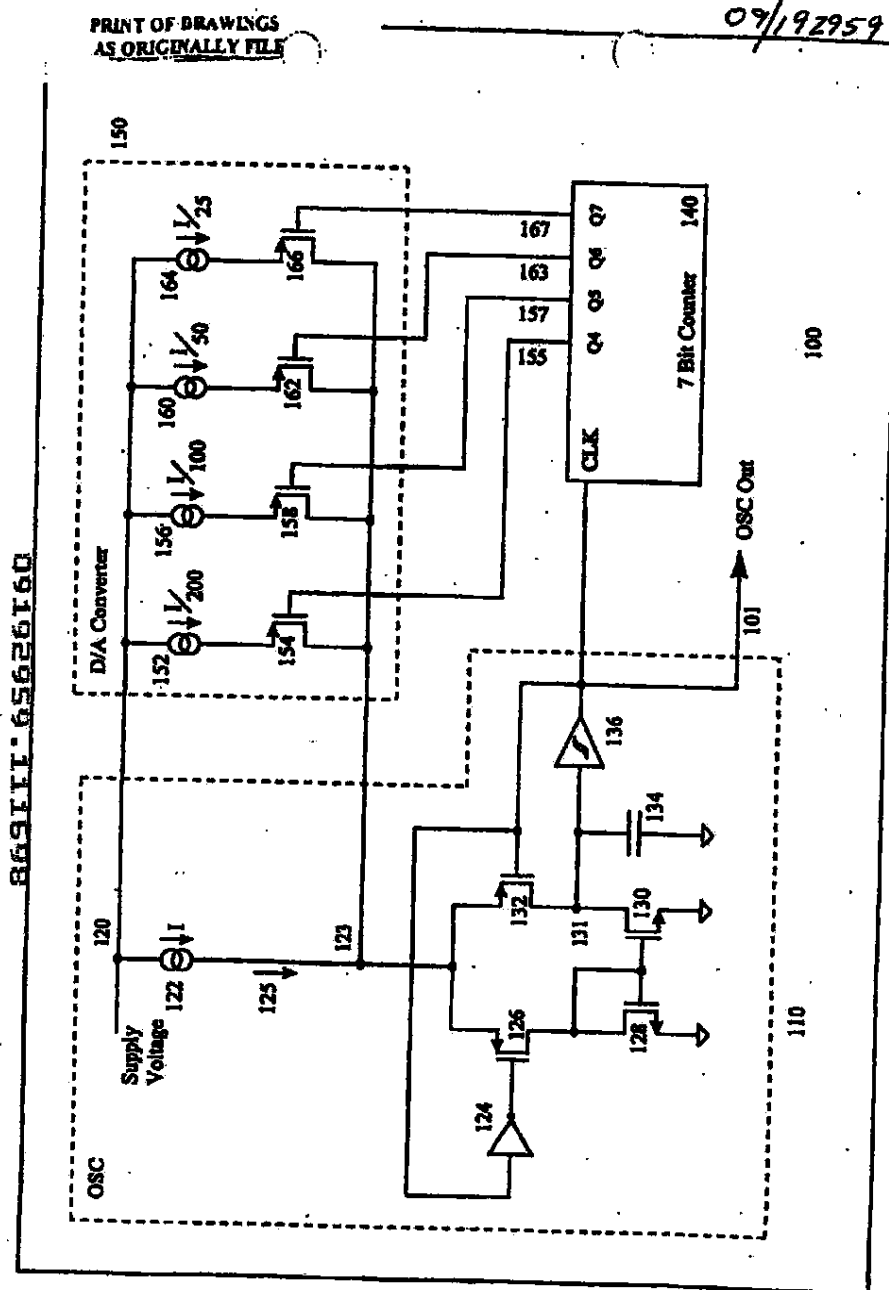


Figure 1.

PRINT OF DRAWINGS  
AS ORIGINALLY FILED

869TTF-65626160

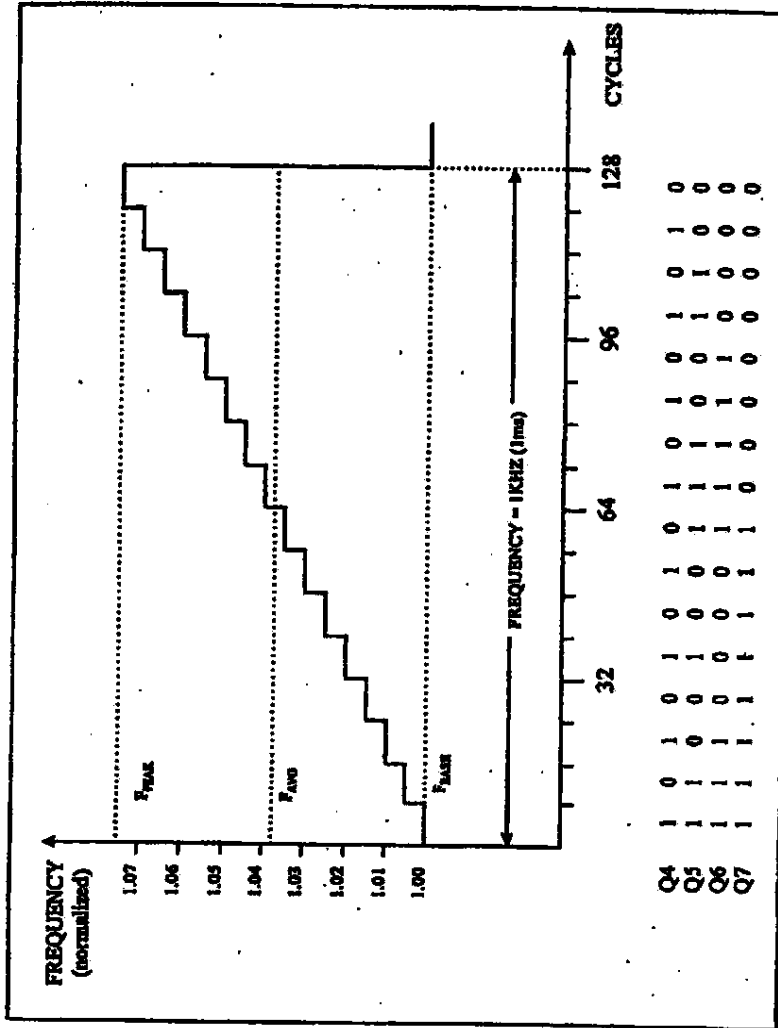


Figure 2.

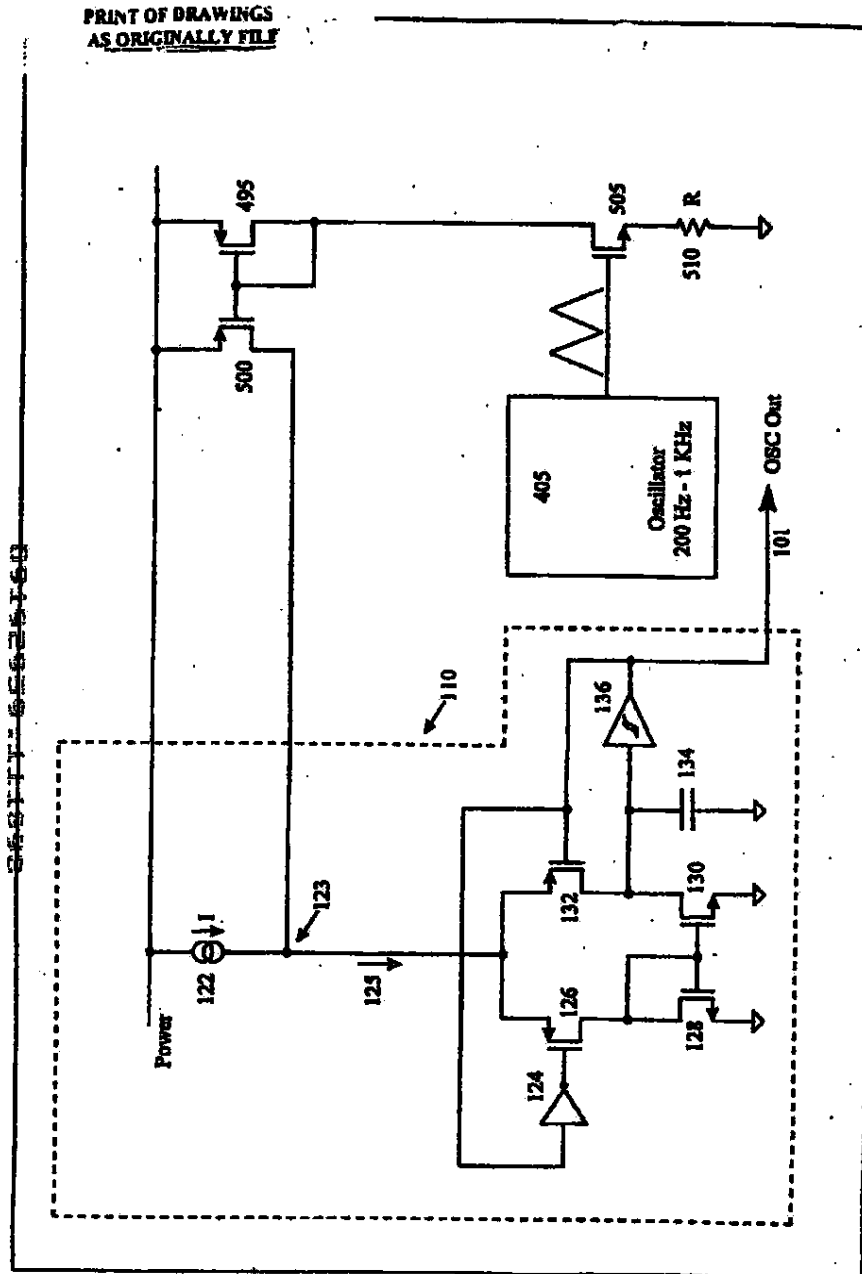


Figure 3.

FCS0000058

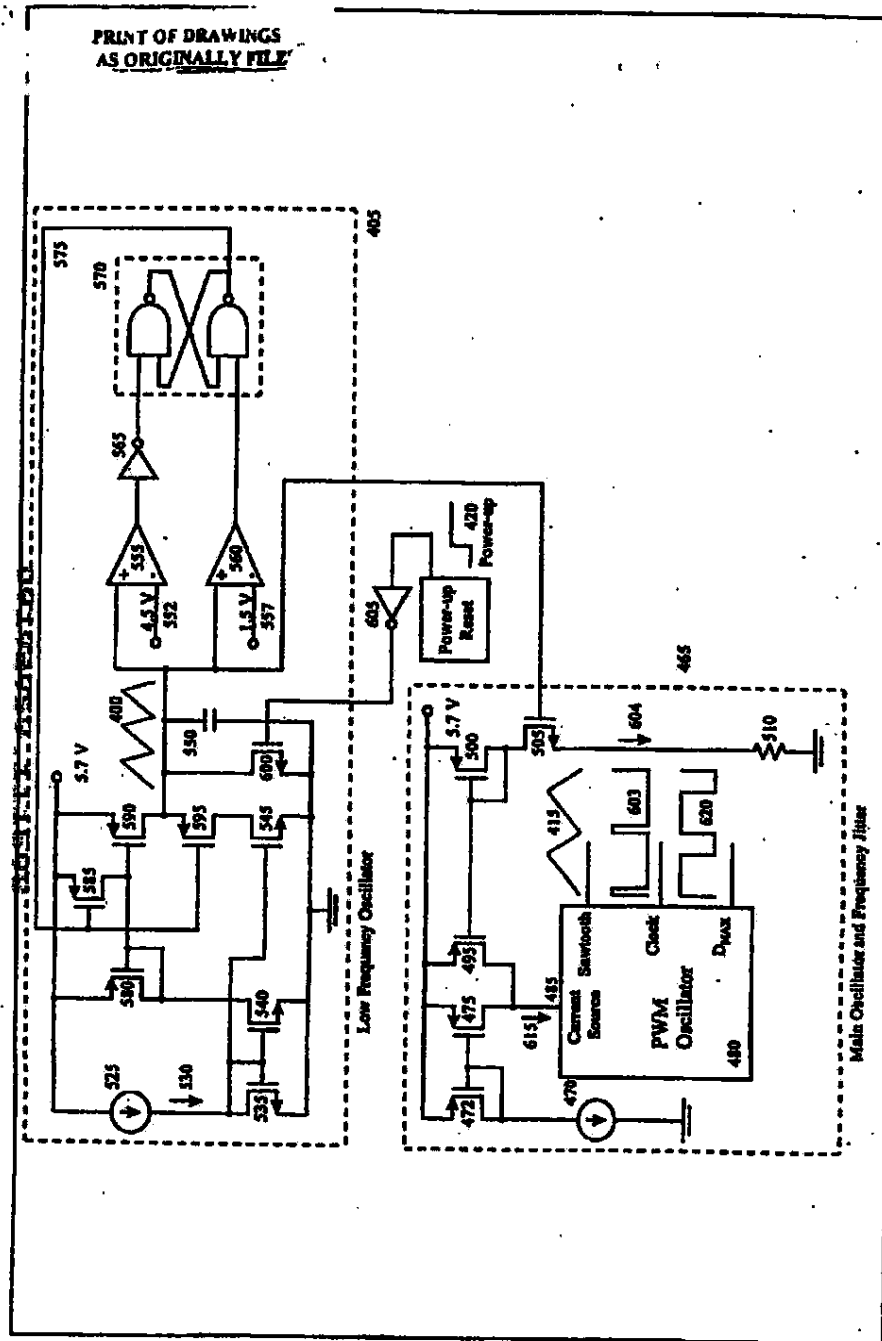


Figure 4.

PRINT OF DRAWINGS  
AS ORIGINALLY FILED

869111-65626160

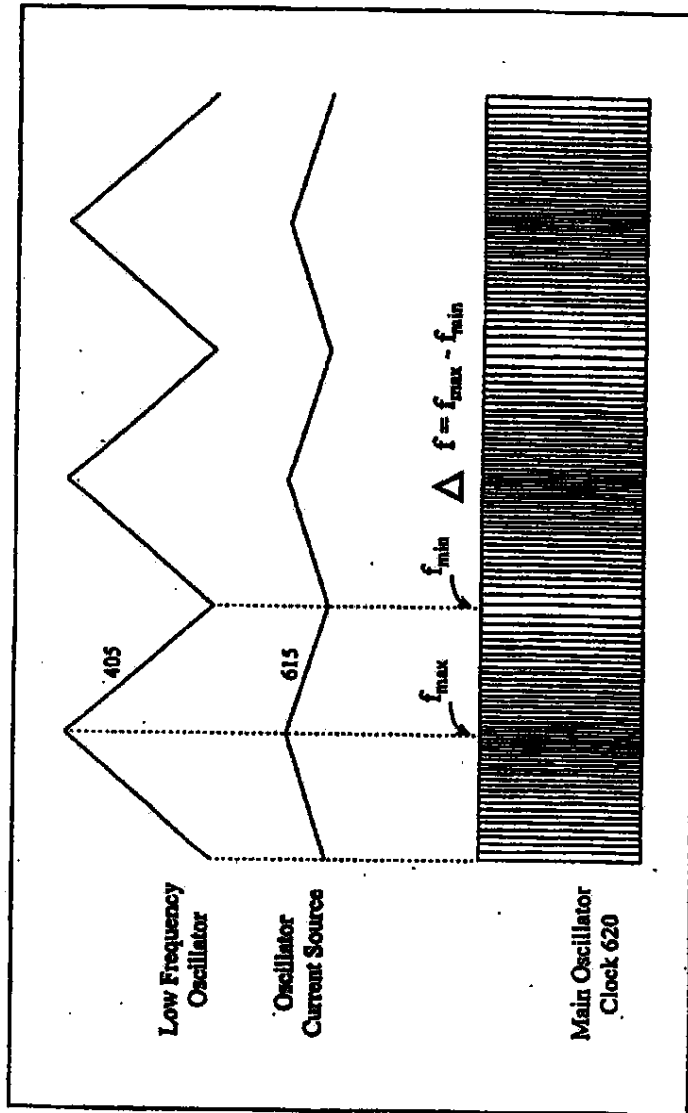
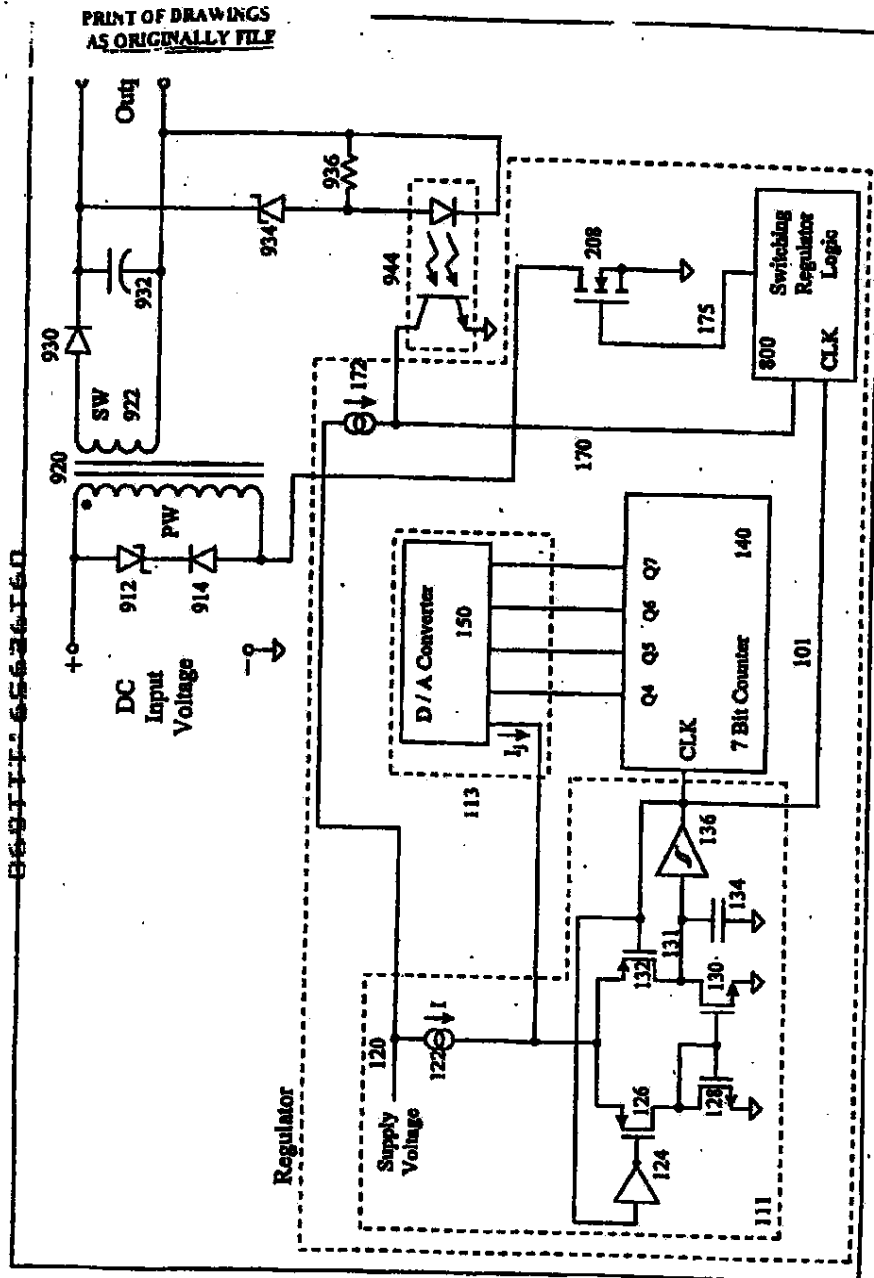


Figure 5.

FCS0000060



**gambit**





ATTORNEY'S LOCKET NO. 10256/003001  
PATENT  
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : B. Balakrishnan et al. Art Unit: Unassigned  
Serial No.: Unassigned Examiner: Unassigned  
Filed : Herewith  
Title : FREQUENCY JITTERING CONTROL

Assistant Commissioner for Patents  
Washington, DC 20231

INFORMATION DISCLOSURE STATEMENT

Applicants submit the references listed on the attached form PTO-1449, copies of which are enclosed.

The Examiner is requested to make these citations of official record in this application. Applicants would appreciate the Examiner initialling and returning an initialled copy of form PTO-1449, indicating that the references have been considered and made of record herein.

This statement is being filed with the application.

Please apply any charges or credits to Deposit Account  
06-1050.

Respectfully submitted,

Date: 11/16/98

Bao Q. Tran  
Bao Q. Tran  
Reg. No. 37,955

Fish & Richardson P.C.  
2200 Sand Hill Road, Suite 100  
Menlo Park, CA 94025

Telephone: 650/322-5070  
Facsimile: 650/854-0875  
26763.FAL1

\*EXPRESS MAIL\* Mailing Label Number EL1105185245  
Date of Deposit 11/16/98

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[illegible]

Substitute Disclosure form (PTO-1449)

**TECH INSIGHT**  
PRODUCT INNOVATION

## Power-Conversion Chip Cuts Energy Wastage In Off-Line Switchers

*High-Voltage Controller Enables Energy-Efficient, Economical Alternatives To AC Wall Adapters And Standby Power Supplies.*

**Ashek Bindra**

**W**hile the efficiencies of power-conversion chips and power sources continue to improve, energy wastage in stand-by mode remains astonishingly high. For example, ac wall adapters are still plugged in and consume power, even though gadgets like TVs, VCRs, and cordless phones are supposedly off. And, the problem is expected to worsen as more electronic consumer products pervade the home.

This wasted energy costs money, as well as contributes to pollution. According to a study conducted by Lawrence Berkeley National Laboratory, Berkeley, Calif., in the U.S. alone, consumers pay over \$3.5 billion annually to keep a variety of electronic widgets in stand-by mode. To curb such wastage, several energy-saving guidelines have been established around the world. The U.S. Energy Star program, for example, has been extended to consumer electronics, with efforts underway to cover home audio and DVD players. Likewise, Germany's Blue Angel legislation is

catching momentum in Europe.

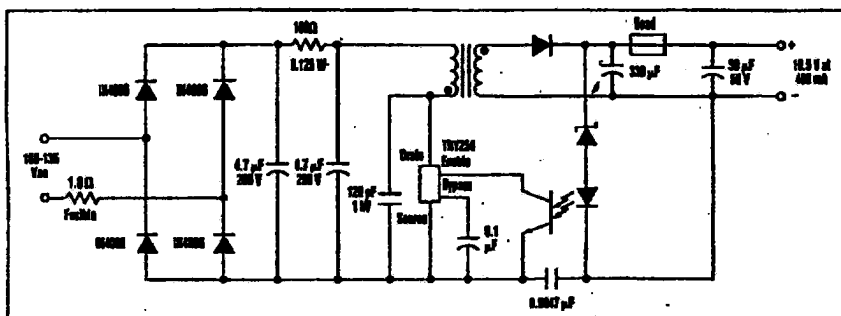
To enable a new class of energy-efficient off-line ac adapters and standby power supplies, Power Integrations Inc. has crafted a radically new switcher solution for low-power (10 W and below) applications (Fig. 1). And, at the heart of this solution is a proprietary controller chip called TinySwitch.

"This new design reduces the energy wastage from the 1.2 W (typical) seen in today's conventional, linear, ac wall adapters (or bricks) to less than 100 mW," says Shyam Dujari, director of marketing at Power Integrations. Plus, he adds, it provides a compact, light-weight adapter or stand-by supply with universal input. Because fewer low-cost external components are needed with this solution, the total system cost is also significantly cut, notes Dujari. By comparison, pulse-width-modulated (PWM) based off-line switchers are bulky and cost more, according to Dujari.

Designed to be a simple, on/off control device, the TinySwitch integrates

on-chip a 700-V power MOSFET; oscillator; high-voltage, switched-current source; current limit; and thermal shutdown circuitry (Fig. 2). Unlike the conventional PWM controller, it uses an on/off control to regulate the output voltage. In this scheme, when the on-chip oscillator is enabled, it turns the power MOSFET on at the start of each cycle. The MOSFET is turned-off as soon as the output current reaches the upper limit.

The maximum on-time of the power MOSFET is determined by the duty cycle signal ( $D_{MAX}$ ) of the internal oscillator. Also, the current limit and switching frequency for a given TinySwitch is fixed, while the power delivered is proportional to the primary inductance of the transformer. Because the TinySwitch is powered directly by the incoming high voltage, it eliminates the need for an auxiliary bias winding and associated circuitry, thereby simplifying the design of the transformer. In fact, the manufacturer recommends standard, low-cost transformers based on ferrite cores like



1. As shown in the application circuit, the TinySwitch requires very few external components to complete a 4-W, off-line ac adapter. The output power is proportional to the primary inductance of the transformer, and is independent of the input voltage.

ELECTRONIC DESIGN / OCTOBER 1, 1998

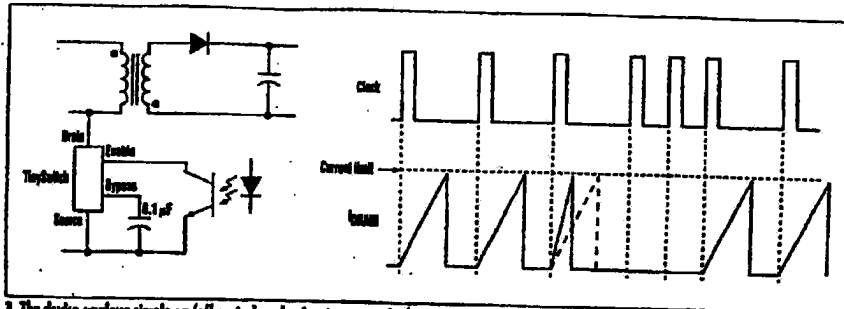
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Cited in IDS for 10256/003001  
Serial No. Unassigned, filed 11/19/08

AA

FCS0000065

## TECH SIGNS EFFICIENT POW CONVERTER



3. The device employs simple on/off control mechanism to operate in the current limit mode, so that it can deliver the same energy every cycle. The current-limit operation rejects line-frequency ripple. The current limit and clock cycle for each device is fixed.

EE16, which is available from multiple sources.

#### Novel Operation

The very-high loop bandwidth of the device provides excellent transient response and fast turn-on, with practically no overshoot, claims Dujari. As per the data sheets, the turn-on time is about 1.0 ms at no load. Plus, he adds, the fixed current-limit operation rejects the line ripple, as the energy delivered is independent of the input voltage (Fig. 3). Other features include glitch-free output when the input is removed, and thermal protection. No loop compensation is needed. The thermal shutdown threshold is set at 135°C, with 70°C hysteresis. Consequently, when the junction temperature exceeds 135°C, the power MOSFET is disabled. It remains disabled

until the die-junction temperature goes under 70°C, at which point it is re-enabled.

Under no-load condition, the TinySwitch consumes only 30 to 60 mW at 115/250-V ac input. As a result, stand-by supplies based on the TinySwitch can meet Blue Angel, Energy Star, Energy 2000, and European cellular phone standards. This smart integration of a high-voltage MOSFET switch with low-voltage control and protection functions is made possible by the company's proprietary CMOS process.

The TNY253/254/255 are the first three members of the TinySwitch family. Aimed at TV/VCR stand-by solutions, the TNY253 is rated for 5-W supplies. Likewise, TNY254 delivers up to 8 W for cellular phone chargers and PC stand-by supplies. Both the

TNY253 and TNY254 switch at 44 kHz to minimize EMI filtering requirements, and permit the use of a simple snubber clamp to limit drain spike voltage.

However, the TNY255 uses a higher switching frequency of 130 kHz to deliver up to 10 W for applications like cell phone chargers and PC stand-by power. All three units allow the use of low-cost, EE16 core transformers. Typical conversion efficiency offered by a TinySwitch-based power converter is 70%-to-75%.

"The efficiency is constant all the way down to very-low power," states Power Integrations' vice president of engineering, Balu Balakrishnan. In PWM-based switchers, the losses stay fixed, as a result, the efficiency goes down with load, Balakrishnan says. By comparison, he adds, the TinySwitch skips cycles at low load to keep the switching losses lower and efficiency higher.

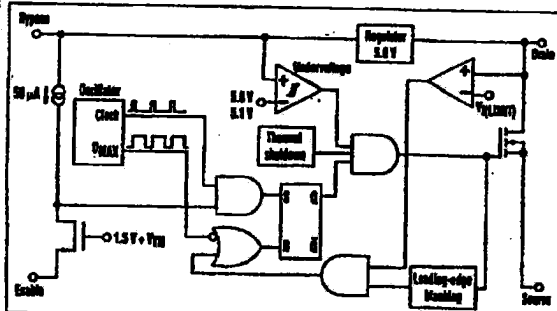
To simplify using TinySwitch devices in power-supply applications, Power Integration's engineers have readied several reference designs and application notes. These include a 1.5-W TV/VCR stand-by circuit, an 8-W PC stand-by supply, and a 3.5-W cellular phone charger. In addition, there is a 0.5-W off-line ac adapter. Evaluation boards are also available for these applications.

#### PRICE AND AVAILABILITY

The TinySwitch TNY252/253/255 devices are available in 8-pin DIP and 8-pin SMD packages. In 10,000-piece quantities, the prices range from \$0.75 to \$0.81 each.

Power Integrations Inc., 177 N. Mathilda Ave., Sunnyvale, CA 91088; (408) 525-9285; [www.powerint.com](http://www.powerint.com)

CIRCLE 451



2. This functional block diagram shows that the TinySwitch controller packs an oscillator, enable circuit, 5.8-V regulator, under-voltage circuit, hysteresis over-temperature protection, current limit, leading-edge blanking, and a 700-V lateral power MOSFET. This is made possible by the semiconductor supplier's proprietary 3.0 µm single metal CMOS process.

ELECTRONICS/NOVEMBER 1, 1998

FCS0000067



Receipt

PATENT  
ATTORNEY DOCKET NO. 10256/003001

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Balakrishnan et al.  
Serial No.: 09/192,959  
Filed : November 16, 1998  
Title : FREQUENCY JITTERING CONTROL  
Assistant Commissioner for Patents  
Washington, DC 20231

Art Unit: 2781  
Examiner: Unassigned

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MAR 09 1999

PETITION TO CORRECT FILING RECEIPT Group 2700

Applicants request that the name of the second inventor on the Filing Receipt be corrected to read: ALEX DJENGUERIAN.

A copy of the Filing Receipt with the correction in red is attached. Applicants request a filing receipt with the above-noted correction.

Please apply any charges not covered, or any credits, to Deposit Account 06-1050.

Respectfully submitted,

Date: 2/19/99 Bao Tran

Bao Q. Tran  
Reg. No. 37,955

Fish & Richardson P.C.  
2200 Sand Hill Road, Suite 100  
Menlo Park, CA 94025

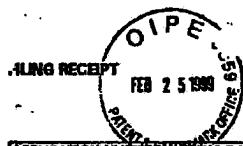
Telephone: 650/322-5070  
Facsimile: 650/854-0875

103840.PAL1

Date of Deposit 22 Feb 99  
I hereby certify under 37 CFR 1.8(a) that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage on the date indicated above and is addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

Long Pawan

FCS0000068



UNITED STATES DEPARTMENT OF COMMERCE  
Patent and Trademark Office  
ASSISTANT SECRETARY AND COMMISSIONER  
OF PATENTS AND TRADEMARKS  
Washington, D.C. 20231

APPLICATION NUMBER	FILING DATE	GRP ART UNIT	FILE REC'D	ATTORNEY DOCKET NO.	DRWGS	TOT CL	IND CL
09/192,959	11/16/98	2781	\$1,246.00	10256/003001	6	34	6

ROGER S BOROVVOY  
FISH & RICHARDSON  
2200 SAND HILL ROAD  
SUITE 100  
MENLO PARK CA 94025

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GPO 2700

Receipt is acknowledged of this nonprovisional Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please write to the Application Processing Division's Customer Connection Branch within 10 days of receipt. Please provide a copy of the Filing Receipt with the changes noted thereon.

Applicant(s)

BALU BALAKRISHNAN, SARATOGA, CA; ALEX DIENGUERIAN,  
SARATOGA, CA; LEIF LUND, SAN JOSE, CA

FOREIGN FILING LICENSE GRANTED 12/02/98

TITLE  
FREQUENCY JITTERING CONTROL

PRELIMINARY CLASS: 395

Docketed By Practice Systems	
Action Code:	CORRECT OFF
Base Date:	12/19/98
Due Date:	1/9/99
Deadline:	
Initials:	LL
Record:	

Docketed By Billing Secretary	
Due Date:	1/19/99
Deadline:	1/19/99
Initials:	RR

DATA ENTRY BY: SMITH ANNETTE

TEAM: 04 DATE: 12/02/98

(see reverse)

FCS0000069





Attorney's Docket No.: 003692.P033



Patent

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:

**BALAKRISHNAN, ET AL**

Application Number: 09/192,959

Filed: November 16, 1998

For: FREQUENCY JITTERING CONTROL

Examiner: Not Yet Assigned

Group Art Unit: 2781

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MAY 27 1999

Group 2700

Assistant Commissioner for Patents  
Washington, D.C. 20231

POWER OF ATTORNEY BY ASSIGNEE  
AND REVOCATION OF PREVIOUS POWERS

Power Integrations, Inc. ("assignee"), a California corporation having a place of business at 477 N. Mathilda Avenue, Sunnyvale, California, 94086, certifies that to the best of assignee's knowledge and belief it is the assignee of the entire right, title, and interest in and to the above-referenced patent application and represents that the undersigned is a representative authorized and empowered to sign on behalf of the assignee.

Assignee has reviewed the assignment document that evidences the placement of title in the assignee and upon information and belief that assignment documents were recorded in the U.S. Patent and Trademark Office on November 16, 1998, at reel 9593, frame 0048.

Pursuant to 37 C.F.R. §§ 1.36 and 3.71, the assignee hereby revokes all powers of attorney previously given and appoints Farzad E. Amini, Reg. No. P42,261; Aloysius T. C. AuYeung, Reg. No. 35,432; Amy M. Armstrong, Reg. No. 42,265; William Thomas Babbitt, Reg. No. 39,591; Carol F. Barry, Reg. No. 41,600; Jordan Michael Becker, Reg. No. 39,602; Bradley J. Bereznak, Reg. No. 33,474; Michael A. Bernadecou, Reg. No. 35,934; Roger W. Blakely, Jr., Reg. No. 25,831; Gregory D. Caldwell, Reg. No. 39,926; Kent M. Chen, Reg. No. 39,630; Yong S. Choi, Reg. No. P43,324; Thomas M. Coester, Reg. No. 39,637; Michael Anthony DeSanctis, Reg. No. 39,957; Daniel M. De Vos, Reg. No. 37,813; Robert Andrew Diehl, Reg. No. 40,992; Tarek N. Fahmi, Reg. No. 41,402; James Y. Go, Reg. No. 40,621; Dinu Gruia, Reg. No. P42,996; David R. Halvorson, Reg. No. 33,395;

003692.P033

- 1 -

(Rev. 5/99)

FCS0000071

Thomas A. Hassing, Reg. No. 36,159; Phuong-Quan Hoang, Reg. No. 41,839; Willmore F. Holbrow III, Reg. No. P41,845; George W. Hoover II, Reg. No. 32,992; Eric S. Hyman, Reg. No. 30,139; Dag H. Johansen, Reg. No. 36,172; William W. Kidd, Reg. No. 31,772; Michael J. Mallie, Reg. No. 36,591; Andre L. Marais, under 37 C.F.R. § 10.9(b); Paul A. Mendonsa, Reg. No. 42,879; Darren J. Milliken, Reg. No. 42,004; Thinh V. Nguyen, Reg. No. 42,034; Kimberley G. Nobles, Reg. No. 38,255; Babak Redjaian, Reg. No. 42,096; James H. Salter, Reg. No. 35,668; William W. Schaal, Reg. No. 39,018; James C. Scheller, Reg. No. 31,195; Anand Sethuraman, Reg. No. P43,351; Charles E. Shemwell, Reg. No. 40,171; Maria McCormack Sobrino, Reg. No. 31,639; Stanley W. Sokoloff, Reg. No. 25,128; Judith A. Szepesi, Reg. No. 39,393; Vincent P. Tassinari, Reg. No. 42,179; Edwin H. Taylor, Reg. No. 25,129; George G. C. Tseng, Reg. No. 41,355; Lester J. Vincent, Reg. No. 31,460; John Patrick Ward, Reg. No. 40,216; Stephen Warhola, Reg. No. 43,237; Charles T. J. Weigell, Reg. No. 43,398; Ben J. Yorks, Reg. No. 33,609; and Norman Zafman, Reg. No. 26,250; my attorneys, and James A. Henry, Reg. No. 41,064; Daniel E. Ovanezian, Reg. No. 41,236; Glenn E. Von Tersch, Reg. No. 41,364; and Chad R. Walsh, Reg. No. 43,235; my patent agents, of BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP, with offices located at 12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 90025, telephone (310) 207-3800, and James R. Thein, Reg. No. 31,710, my patent attorney; with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

Pursuant to 37 C.F.R. § 3.71, the assignee hereby states that prosecution of the above-referenced patent application is to be conducted to the exclusion of the inventor(s).

Send all future correspondence to Bradley J. Bereznek, Esq., Reg. No. 33,474, Blakely, Sokoloff, Taylor, & Zafman LLP, 12400 Wilshire Boulevard, Seventh Floor, Los Angeles, California 90025, and direct all telephone calls to the same at (408) 720-8598.

Assignee of Interest: POWER INTEGRATIONS, INC.  
(Type or Print)

Dated: 5-14-99

By:   
Name: Clifford J. Walker  
(Type or Print)

Title: Vice President of Corporate Development  
(Type or Print)

Address of Assignee of Interest:  
477 N. Mathilda Avenue  
Sunnyvale, CA 94086  
USA

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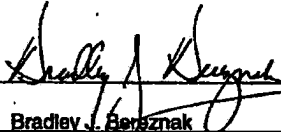
- 2 -

(Rev. 5/99)

FCS0000072

Respectfully submitted,

**BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP**

Dated: 5/17/99 By   
Name: Bradley J. Berzjak  
(Type)  
Reg. No.: 33,474

12400 Wilshire Blvd.  
Seventh Floor  
Los Angeles, California 90025-1026  
(408) 720-8598

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**MAY 27 1999**  
Group 2700

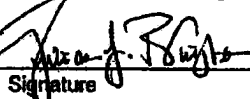
**FIRST CLASS CERTIFICATE OF MAILING**  
**(37 C.F.R. § 1.8(a))**

I hereby certify that the foregoing Power of Attorney is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231 on

May 17, 1999

Vivian Y. Buijten

Name of Person Mailing Correspondence

  
Signature

5/17/99  
Date





UNITED STATES DEPARTMENT OF COMMERCE  
Patent and Trademark Office  
Address: COMMISSIONER OF PATENTS AND TRADEMARKS  
Washington, D.C. 20231

SERIAL NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.
---------------	-------------	-----------------------	---------------------

09/192969 11/16/98 BALAKRISHNAN

10256/003001  
EXAMINER

ROGER S. BOROVY  
FISH & RICHARDSON  
2200 SAND HILL ROAD  
SUITE 100  
MENLO PARK CA 94025

ASSISTANT  
SHELDON AVAZZ PAPER NUMBER

DATE MAILED

06/01/99

This is in response to the Power of Attorney filed \_\_\_\_\_

- ☐ 1. The Power of Attorney to you in this application has been revoked by the applicant. Future correspondence will be mailed to the new address of record. 37 CFR 1.33.
- ☒ 2. The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record. (37 CFR 1.33).
- ☐ 3. The withdrawal as attorney in this application has been accepted. Future correspondence will be mailed to the new address of record. 37 CFR 1.33.

*[Signature]*  
This is a communication from the  
Patent and Trademark Office

- ☒ 4. The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the below-noted address as provided by 37 CFR 1.33.
- ☐ 5. The Power of Attorney in this application is not accepted for the reason(s) checked below:
- ☐ a. The Power of Attorney is from an assignee and the Certificate required by 37 CFR 3.73 (b) has not been received.
  - ☐ b. The person signing for the assignee has omitted their empowerment to sign on behalf of the assignee.
  - ☐ c. The inventor(s) is without authority to appoint attorneys since the assignee has intervened as provided by 37 CFR 3.71.
  - ☐ d. The signature of \_\_\_\_\_, a co-inventor in this application, has been omitted. The Power of Attorney will be entered upon receipt of confirmation signed by said co-inventor.
  - ☐ e. The person(s) appointed in the Power of Attorney is not registered to practice before the U. S. Patent & Trademark Office.
  - ☐ f. The revocation is not signed by the applicant, the assignee of the entire interest, or one particular principal attorney having the authority to revoke.

BRADLEY J. BEREZNAK, ESQ.  
BLAKELY SOKOLOFF TAYLOR & ZAFMAN, LLP  
12400 WILSHIRE BLVD.  
SEVENTH FLOOR  
LOS ANGELES CA 90025

*[Signature]*  
This is a communication from the  
Patent and Trademark Office





UNITED STATES DEPARTMENT OF COMMERCE  
Patent and Trademark Office  
Address: COMMISSIONER OF PATENTS AND TRADEMARKS  
Washington, D.C. 20231

APPLICATION NUMBER	FILED DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.
09/192,959	11/16/98	BALAKRISHNAN	B 10256/003001

TM11/1016

BRADLEY J. BEREZNAK, ESQ.  
BLAKELY SOKOLOFF TAYLOR & ZAFMAN, LLP  
12400 WILSHIRE BLVD.  
SEVENTH FLOOR  
LOS ANGELES CA 90025

EXAMINER	
RUTLER, D	
ART UNIT	PAPER NUMBER
2182	6

DATE MAILED: 10/16/00

This is a communication from the examiner in charge of your application.  
COMMISSIONER OF PATENTS AND TRADEMARKS

#### OFFICE ACTION SUMMARY

☒ Responsive to communication(s) filed on 11-16-98

☐ This action is FINAL.

☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 D.C. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire three month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

#### Disposition of Claims

☒ Claim(s) 1-34 is/are pending in the application.

Of the above, claim(s) \_\_\_\_\_ is/are withdrawn from consideration.

☒ Claim(s) 1-10 is/are allowed.

☒ Claim(s) 11-13, 17-18, 21, 27-28 and 31-34 is/are rejected.

☒ Claim(s) 14-16, 19-20, 22-26 and 29-30 is/are objected to.

☐ Claims \_\_\_\_\_ are subject to restriction or election requirement.

#### Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on \_\_\_\_\_ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on \_\_\_\_\_ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

#### Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) \_\_\_\_\_

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

\*Certified copies not received: \_\_\_\_\_

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

#### Attachment(s)

☒ Notice of Reference Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). 2

☐ Interview Summary, PTO-413

☒ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

- SEE OFFICE ACTION ON THE FOLLOWING PAGES -

PTOL-328 (Rev. 10/95)

U.S. GPO: 1996-418-240-00028

FCS0000077



Serial Number J9/192,959  
Art Unit 2787

- 2 -

1. This action is in response to the application filed on November 16, 1998. Claims 1-34 are pending.
2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The current title is imprecise. The title would be improved if it included that the frequency jittering control is for varying the switching frequency of a power supply.
3. Claims 27-28 and 32-34 are rejected under 35 USC 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claims 27-28, the phrase "the primary current source" lacks proper antecedent basis. The phrase "the current sources" lacks proper antecedent basis and is unclear because it is unclear whether it refers to all the current sources including the primary current source or just the one or more current sources coupled to the control input.

Regarding claim 32, the phrase "the means for ... the capacitor" lacks proper antecedent basis and is unclear as to its relationship to the current source adapted to charge and discharge the capacitor.

Regarding claim 33, the phrase "the analog to digital converter" lacks proper antecedent basis. The phrase "the current sources" lacks proper antecedent basis and is unclear because it is unclear whether it refers to all the current sources including the primary current source or just the one or more current

FCS0000078

Serial Number J9/192,959  
Art Unit 2787

- 3 -

sources coupled to the control input.

Regarding claim 34, the phrase "comparators coupled to the capacitor to the current source" is unclear as to the coupling of the comparators.

4. The following is a quotation of the appropriate paragraphs of 35 USC § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. This application currently names joint inventors. In considering patentability of the claims under 35 USC 103, the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of potential 35 USC 102(f) or (g) prior art under 35 USC 103.

6. The following is a quotation of 35 USC 103 which forms the basis for all obviousness rejections set forth in this Office action:

A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Subject matter developed by another person, which qualifies as prior art only under subsection (f) or (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

7. Claims 11, 13, 17, 21 and 31-32 rejected under 35 USC 102(b)

FCS0000079

Serial Number J9/192,959  
Art Unit 2787

- 4 -

as being anticipated by Albach, U.S. Patent 4,712,169.

Per claims 11, 13 and 17:

A) Albach teaches the following claimed items:

1. generating a primary current/voltage with Uref of figure 1, at column 4, lines 13-15 and at column 5, lines 38-47;
2. cycling one or more secondary current/voltage sources to generate a secondary current/voltage which varies over time with U1 of figures 1 and 2, at column 4, lines 10-15 and at column 4, line 57 - column 5, line 8;
3. supplying the primary and secondary currents/voltages to a control input of an oscillator (VCO 34) for generating a switching frequency which varies over time with U2 of figures 1 and 2, at column 4, lines 15-26 and at column 5, lines 9-66.

Per claims 21 and 31-32:

A) Albach teaches the following claimed items:

1. an oscillator with VCO 34 of figure 1, at column 4, lines 15-26 and 41-61;
  2. means for varying the switching frequency including a capacitor, a current source and a comparator with comparator circuit 31, monostable trigger 32 and integrator 33 of figure 1, at column 4, lines 7-26.
8. Claims 12 and 18 rejected under 35 USC 103 as being unpatentable over Albach, U.S. Patent 4,712,169.

The claims seem to differ from Albach in that Albach fails to explicitly teach clocking a counter with the output of the oscillator as claimed. However, Albach describes

FCS0000080

Serial Number 09/192,959  
Art Unit 2787

- 5 -

clocking SR Latch 26 of figure 1 and at column 4, lines 20-26 in order to condition the output of the oscillator for the switching transistor. Albach does not explicitly describe using a counter to condition the oscillator output signal. However, counters are routinely used as frequency dividers in order to generate the desired frequency for the receiving device. It would have been obvious to one having ordinary skill in the data processing art at the time the invention was made to replace the SR latch with a counter in order to increase the flexibility of the pulse generating circuit by allowing the oscillator frequency to be divided down to a lower frequency and properly condition the oscillator output to the proper switching frequency.

9. Claims 1-10 are allowable over the art of record.

10. Claims 14-16, 19-20, 22-26 and 29-30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dennis M. Butler whose telephone number is (703) 305-9663. The examiner can normally be reached on Monday-Friday from 9:30 AM to 6:00 PM.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Dennis M. Butler  
October 10, 2000

*Dennis M. Butler*  
Dennis M. Butler  
Primary Examiner  
Group 2180

FCS0000081

FORM PTO 948 (REV. 11-97)

U.S. DEPARTMENT OF COMMERCE-Patent and Trademark Office

Application No.

192959

NOTICE OF DRAFTPERSON'S  
PATENT DRAWING REVIEW

The drawing filed (insert date) \_\_\_\_\_

A. \_\_\_\_\_ not objected to by the Draftperson under 37 CFR 1.84(a) or 1.152(a) (1) or (2) of the Manual of Patent Examining Procedure.

B. \_\_\_\_\_ objected to by the Draftperson under 37 CFR 1.84 or 1.152 as indicated below. The Examiner will require submission of new, corrected drawings, where necessary. Corrected drawings must be submitted according to the instructions on the back of this notice.

## 1. DRAWINGS. 37 CFR 1.84(a): Acceptable categories of drawings.

Black ink. Color.

Color drawings are not acceptable until position is granted.

Fig.(s) \_\_\_\_\_

Pencil and non black ink is not permitted. Fig.(s) \_\_\_\_\_

## 2. PHOTOGRAPHS. 37 CFR 1.84(b)

Photographs are not acceptable until position is granted.

3 full-tone sets are required. Fig.(s) \_\_\_\_\_

Photographs not properly mounted (must be on board or photographic double-weight paper). Fig.(s) \_\_\_\_\_

Four quality (half-tone). Fig.(s) \_\_\_\_\_

## 3. TYPE OF PAPER. 37 CFR 1.84(c)

Paper not flexible, strong, white and durable.

Fig.(s) \_\_\_\_\_

## 4. SIZE OF PAPER. 37 CFR 1.84(d): Acceptable size.

21.6 cm by 27.9 cm (8 1/2 x 11 inches)

21.6 cm by 27.9 cm (8 1/2 x 11 inches)

All drawings sheets not the same size.

Sheet(s) \_\_\_\_\_

## 5. MARGINS. 37 CFR 1.84(e): Acceptable margins.

Top 2.5 cm Left 2.5 cm Right 1.5 cm Bottom 1.0 cm

SIZE: A4 Size

Top 2.5 cm Left 2.5 cm Right 1.5 cm Bottom 1.0 cm

SIZE: 8 1/2 x 11

Margins not acceptable. Fig.(s) \_\_\_\_\_

Top (T) \_\_\_\_\_ Left (L) \_\_\_\_\_

Right (R) \_\_\_\_\_ Bottom (B) \_\_\_\_\_

## 6. VIEWS. 37 CFR 1.84(f)

REMINDER: Specification may require revision to correspond to drawing changes.

11. Views connected by projection lines or lead lines.

Fig.(s) \_\_\_\_\_

Partial views. 37 CFR 1.84(g)(2)

Brackets needed to show figure as one entity.

Fig.(s) \_\_\_\_\_

Views not labeled separately or properly.

Fig.(s) \_\_\_\_\_

Enlarged view not labeled separately or properly.

Fig.(s) \_\_\_\_\_

## 7. SECTIONAL VIEWS. 37 CFR 1.84(h)(3)

Hatching not indicated for sectioned portions of an object.

Fig.(s) \_\_\_\_\_

Sectional designation should be noted with Arabic or Roman numbers. Fig.(s) \_\_\_\_\_

## 8. ARRANGEMENT OF VIEWS. 37 CFR 1.84(i)

Views do not appear on a horizontal, left-to-right fashion when page is either upright or turned, so that the top becomes the right side, except for graphs. Fig.(s) \_\_\_\_\_

## 9. SCALE. 37 CFR 1.84(j)

Scale not large enough to show mechanism without crowding when drawing is reduced in size to two-thirds in reproduction.

Fig.(s) \_\_\_\_\_

## 10. CHARACTER OF LINES, NUMBERS, &amp; LETTERS. 37 CFR 1.84(k)

Lines, numbers &amp; letters not uniformly thick and well defined, clear, double and black (near line quality).

Fig.(s) \_\_\_\_\_

## 11. SHADING. 37 CFR 1.84(l)

Solid black areas pale. Fig.(s) \_\_\_\_\_

Solid black shading not permitted. Fig.(s) \_\_\_\_\_

Shade lines, pale, rough and blurred. Fig.(s) \_\_\_\_\_

## 12. NUMBERS, LETTERS, &amp; REFERENCE CHARACTERS. 37 CFR 1.84(m)

Numbers and reference characters not plain and legible.

Fig.(s) \_\_\_\_\_

Figure legends are poor. Fig.(s) \_\_\_\_\_

Numbers and reference characters not oriented in the same direction as the view. 37 CFR 1.84(p)(3) Fig.(s) \_\_\_\_\_

English alphabet not used. 37 CFR 1.84(p)(3) Fig.(s) \_\_\_\_\_

Numbers, letters and reference characters must be at least 32 cm (1/8 inch) in height. 37 CFR 1.84(p)(3) Fig.(s) \_\_\_\_\_

## 13. LEAD LINES. 37 CFR 1.84(n)

Lead lines cross each other. Fig.(s) \_\_\_\_\_

Lead lines ending in arrowheads. Fig.(s) \_\_\_\_\_

## 14. NUMBERING OF SHEETS OF DRAWINGS. 37 CFR 1.84(o)

Sheets not numbered consecutively, and in Arabic numerals beginning with number 1. Fig.(s) \_\_\_\_\_

## 15. NUMBERING OF VIEWS. 37 CFR 1.84(p)

Views not numbered consecutively, and in Arabic numerals, beginning with number 1. Fig.(s) \_\_\_\_\_

## 16. CORRECTIONS. 37 CFR 1.84(q)

Corrections not made from PTO 948 dated \_\_\_\_\_

## 17. DESIGN DRAWINGS. 37 CFR 1.152

Surface shading shown not appropriate. Fig.(s) \_\_\_\_\_

Solid black shading not used for color contrast.

Fig.(s) \_\_\_\_\_

COMMENTS

REVIEWER

DATE

TELEPHONE NO.

ATTACHMENT TO PAPER NO.

PTO COPY

FCS0000082

PAGE 1 OF 1

FORM PTO-892		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		SERIAL NO. <b>09/192,959</b>	GROUP ART UNIT <b>2787</b>	ATTACHMENT TO PAPER NO. <b>6</b>
NOTICE OF REFERENCES CITED				APPLICANT(S) <b>Balakrishnan et al.</b>		
U.S. PATENT DOCUMENTS						
*		DOCUMENT NO.	DATE	NAME	CLASS	SUB-CLASS
	A	6,107,851	8/2000	Balakrishnan et al.	327	172
	B	5,459,382	10/1995	Mandelcom	323	222
	C	4,930,063	5/1990	Herze et al.	363	91
	D	4,712,169	12/1987	Albach	363	89
	E					
	F					
	G					
	H					
	I					
	J					
	K					
FOREIGN PATENT DOCUMENTS						
*		DOCUMENT NO.	DATE	COUNTRY	NAME	CLASS
	L					
	M					
	N					
	O					
	P					
	Q					
OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)						
	R					
	S					
	T					
	U					
EXAMINER		DATE				
Dennis M. Butler		October 10, 2000		Form 892oca2106b		
* A copy of this reference is not being furnished with this office action. (See Manual of Patent Examining Procedure, section 707.05(a).)						

FCS0000083

-> d his

(FILE 'HOME' ENTERED AT 14:58:06 ON 06 OCT 2000)

```

FILE 'USPATFULL' ENTERED AT 14:58:19 ON 06 OCT 2000
L1      3 S JITTER### (5A) (SWITCHING FREQUENCY)
L2      9804 S SWITCH### (3W) (POWER SUPPLY)
L3      248428 S OSCILLATOR# OR CLOCK#
L4      3820 S L2 AND L3
L5      999 S REDUC### (5A) EMI
L6      40 S L4 AND L5
L7      173 S VARY### (3A) (SWITCHING FREQUENCY)
L8      537 S CONTROL#### (3A) (SWITCHING FREQUENCY)
L9      2 S L6 AND L7
L10     2 S L6 AND L8
L11     4436 S DIGITAL (W) (ANALOG CONVERTER#)
L12     0 S L6 AND L11
L13     64 S L2 AND L11
L14     40 S L3 AND L13
L15     0 S L14 AND JITTER###
L16     0 S L14 AND (L7 OR L8)
L17     752 S 713/500/NCL OR 713/501/NCL OR 713/503/NCL
L18     793 S 713/300/NCL OR 713/320/NCL OR 713/322/NCL
L19     57 S L17 AND L18
L20     1 S L2 AND L19
L21     0 S L19 AND L5
L22     37 S L6 NOT (L9 OR L10)
L23     1 S L22 AND JITTER###

```

FCS0000084







#7

Attorney's Docket No.: 003882.P033

Patent

In re the Application of: Balakrishnan et al.

(inventor(s))

Application No.: 09/192,959Filed: November 18, 1998For: FREQUENCY JITTERING CONTROL FOR VARYING THE SWITCHING FREQUENCY  
OF A POWER SUPPLY

(title)

ASSISTANT COMMISSIONER FOR PATENTS  
Washington, D.C. 20231

SIR: Transmitted herewith is an Amendment for the above application.

Small entity status of this application under 37 C.F.R. §§ 1.9 and 1.27 has been established by a verified statement previously submitted.

A verified statement to establish small entity status under 37 C.F.R. §§ 1.9 and 1.27 is enclosed.

☒ No additional fee is required.

The fee has been calculated as shown below:

(Col. 1)		(Col. 2)		(Col. 3)	SMALL ENTITY		OTHER THAN A SMALL ENTITY	
	Claims Remaining After Amd.		Highest No. Previously Paid For	Present Extra	Rate	Additional Fee	Rate	Additional Fee
Total Claims	* 32	Minus	** 34	0	X9	\$	X18	\$
Indep. Claims	* 6	Minus	*** 6	0	X40	\$	X80	\$
First Presentation of Multiple Dependent Claim(s)					+135	\$	+270	\$
* If the entry in Col. 1 is less than the entry in Col. 2, write "0" in Col. 3. ** If the "Highest No. Previously Paid For" IN THIS SPACE is less than 20, write "20" in this space. *** If the "Highest No. Previously Paid For" IN THIS SPACE is less than 3, write "3" in this space. The "Highest No. Previously Paid For" (Total or Independent) is the highest number found from the equivalent box in Col. 1 of a prior amendment or the number of claims originally filed.					Total Add. Fee	\$	Total Add. Fee	\$

I hereby certify that this correspondence is being deposited with the United States Postal Service as first-class mail with sufficient postage in an envelope addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231

on January 8, 2001

Date of Deposit

Melanie Bessicker

Name of Person Mailing Correspondence

Signature

1-8-01

Date

- 1 -

(LJV/cak 10/01/00)

FCS0000086

\_\_\_\_\_ A check in the amount of \$ \_\_\_\_\_ is attached for presentation of additional claim(s).  
\_\_\_\_\_ Applicant(s) hereby Petition(s) for an Extension of Time of \_\_\_\_\_ month(s) pursuant to  
37 C.F.R. § 1.136(a).  
\_\_\_\_\_ A check for \$ \_\_\_\_\_ is attached for processing fees under 37 C.F.R. § 1.17.  
\_\_\_\_\_ Please charge my Deposit Account No. 02-2686 the amount of \$ \_\_\_\_\_.  
\_\_\_\_\_ A duplicate copy of this sheet is enclosed.  
\_\_\_\_\_ X The Commissioner of Patents and Trademarks is hereby authorized to charge payment of the  
following fees associated with this communication or credit any overpayment to Deposit Account  
No. 02-2686 (a duplicate copy of this sheet is enclosed):  
\_\_\_\_\_ X Any additional filing fees required under 37 C.F.R. § 1.16 for presentation of  
extra claims.  
\_\_\_\_\_ X Any extension or petition fees under 37 C.F.R. § 1.17.

Date:

1/8/01

12400 Wilshire Boulevard  
Seventh Floor  
Los Angeles, California 90025  
(425) 827-8600

BRADLEY SOKOLOFF TAYLOR & ZAFMAN LLP

James Y. Go

Reg. No. 40,621

2182  
RECEIVED

JAN 22 2001

Attorney's Docket No.: 003692.P033

In re the Application of: Balakrishnan et al.

(Inventor(s))

TC 2100 MAILROOM

Application No.: 09/192,959

Filed: November 18, 1998

For: FREQUENCY JITTERING CONTROL FOR VARYING THE SWITCHING FREQUENCY  
OF A POWER SUPPLY

(Title)

ASSISTANT COMMISSIONER FOR PATENTS  
Washington, D.C. 20231

SIR: Transmitted herewith is an Amendment for the above application.

Small entity status of this application under 37 C.F.R. §§ 1.9 and 1.27 has been established by a verified statement previously submitted.

A verified statement to establish small entity status under 37 C.F.R. §§ 1.9 and 1.27 is enclosed.  
☒ No additional fee is required.

The fee has been calculated as shown below:

(Col. 1)		(Col. 2)		(Col. 3)	SMALL ENTITY		OTHER THAN A SMALL ENTITY	
	Claims Remaining After Amd.		Highest No. Previously Paid For	Present Extra	Rate	Additional Fee	Rate	Additional Fee
Total Claims	32	Minus	34	0	X9	\$	X18	\$
Indep. Claims	6	Minus	6	0	X40	\$	X60	\$
First Presentation of Multiple Dependent Claim(s)					+135	\$	+270	\$
* If the entry in Col. 1 is less than the entry in Col. 2, write "0" in Col. 3. ** If the "Highest No. Previously Paid For" IN THIS SPACE is less than 20, write "20" in this space. *** If the "Highest No. Previously Paid For" IN THIS SPACE is less than 3, write "3" in this space. The "Highest No. Previously Paid For" (Total or Independent) is the highest number found from the equivalent box in Col. 1 of a prior amendment or the number of claims originally filed.					Total Add. Fee	\$	Total Add. Fee	\$

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231

on January 6, 2001

Date of Deposit

Melanie Bessecker

Name of Person Mailing Correspondence

Melanie Bessecker

Signature

1-8-01

Date

RECEIVED  
JAN 19 2001  
TECHNICAL CENTER 2800

- 1 -

(LJV/cak 10/01/00)

FCS0000088

☐ A check in the amount of \$ \_\_\_\_\_ is attached for presentation of additional claim(s).  
☐ Applicant(s) hereby Petition(s) for an Extension of Time of \_\_\_\_\_ month(s) pursuant to 37 C.F.R. § 1.136(a).  
☐ A check for \$ \_\_\_\_\_ is attached for processing fees under 37 C.F.R. § 1.17.  
☐ Please charge my Deposit Account No. 02-2668 the amount of \$ \_\_\_\_\_.  
☐ A duplicate copy of this sheet is enclosed.  
☒ The Commissioner of Patents and Trademarks is hereby authorized to charge payment of the following fees associated with this communication or credit any overpayment to Deposit Account No. 02-2668 (a duplicate copy of this sheet is enclosed):  
☒ Any additional filing fees required under 37 C.F.R. § 1.16 for presentation of extra claims.  
☒ Any extension or petition fees under 37 C.F.R. § 1.17.

Date: 1/8/01  
12400 Wilshire Boulevard  
Seventh Floor  
Los Angeles, California 90025  
(425) 827-8600

BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP

  
James Y. Go

Reg. No. 40,621

003692.P033



Patent

#7/A  
BT

1-23-01

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

BALAKRISHNAN ET AL.

Examiner: D. Butler

Serial No. 09/192,959

Art Unit: 2182

Filed: November 16, 1998

For: FREQUENCY JITTERING CONTROL  
FOR VARYING THE SWITCHING  
FREQUENCY OF A POWER SUPPLY

Box Non Fee Amendment  
Assistant Commissioner for Patents  
Washington, DC 20231

TECHNOLOGY CENTER 2800

JAN 19 2001

-RECEIVED

AMENDMENT AND RESPONSE

Sir:

Responsive to the Office Action mailed October 16, 2000, the Applicants request  
the Examiner to enter the following amendments and to consider the following remarks.

IN THE TITLE

Please change "FREQUENCY JITTERING CONTROL" to --FREQUENCY  
JITTERING CONTROL FOR VARYING THE SWITCHING FREQUENCY OF A  
POWER SUPPLY--.

RECEIVED  
JAN 22 2001  
TIC 2100 HALLROOM

IN THE CLAIMS

Please cancel claims 22 and 29 without prejudice.

003692.P033  
Serial No. 09/192,959

- 1 -

Examiner: D. Butler  
Art Unit: 2182

A

FCS0000090

Please amend claims 11, 17, 21, 23, 26-28, 30, 32, 33 and 34 as follows:

11. (Amended) A method for generating a switching frequency in a power conversion system, comprising:

generating a primary current;

a<sup>1</sup> cycling one or more secondary current sources to generate a secondary current which varies over time; and

[supplying the primary and secondary currents] combining the secondary current with the primary current to be received at a control input of an oscillator for generating a switching frequency which is varied over time.

17. (Amended) A method for generating a switching frequency in a power conversion system, comprising:

generating a primary voltage;

a<sup>2</sup> cycling one or more secondary voltage sources to generate a secondary voltage which varies over time; and

[supplying the primary and secondary voltages] combining the secondary voltage with the primary voltage to be received at a control input of a voltage-controlled oscillator for generating a switching frequency which is varied over time.

21. (Amended) A frequency jittering circuit for varying a power supply switching frequency, comprising:

a<sup>3</sup> an oscillator for generating a signal having a switching frequency, the oscillator having a control input for varying the switching frequency; and

003692.P033  
Serial No. 09/192,959

- 2 -

Examiner: D. Butler  
Art Unit: 2182

21 A  
FCS0000091

means coupled to the control input for varying the switching frequency, including:  
one or more current sources coupled to the control input; and  
a counter coupled to the output of the oscillator and to the one or more current  
sources.

a<sup>3</sup>

a<sup>4</sup> ✓ <sup>22</sup><sub>25</sub>. (Amended) The circuit of claim [22]<sup>22</sup><sub>21</sub> wherein the oscillator further comprises:  
a primary current source coupled to the control input; and  
a differential switch coupled to the primary current source.

<sup>27</sup><sub>26</sub>. (Amended) The circuit of claim [22]<sub>21</sub> further comprising a transistor coupled to  
each current source and to the counter.

a<sup>5</sup> <sup>25</sup><sub>27</sub>. (Amended) The circuit of claim [22]<sup>22</sup><sub>23</sub> wherein the primary current source generates  
a current I and each of [the]said one or more current sources generates a current lower than I.

<sup>26</sup><sub>28</sub>. (Amended) The circuit of claim [22]<sup>22</sup><sub>24</sub> wherein the primary current source generates  
a current I and each of [the]said one or more current sources generates a second current lower  
than the current I, further comprising a transistor coupled to each current source connected to the  
counter.

a<sup>6</sup> <sup>28</sup><sub>29</sub>. (Amended) The circuit of claim [22]<sub>21</sub> wherein the oscillator further comprises:  
a primary voltage source coupled to the control input; and a differential switch coupled to  
the primary voltage source.

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<sup>30</sup>~~32~~ (Amended) The circuit of claim <sup>29</sup>~~31~~ further comprising:

one or more comparators coupled to the capacitor; and

[the] means coupled to the capacitor for alternatingly charging and discharging the capacitor.

<sup>31</sup>~~33~~ (Amended) A power supply having a transformer coupled to an input voltage, the transformer having a primary winding, the power supply comprising:

an oscillator for generating a signal having a frequency, the oscillator having a control input for varying the frequency of the signal, the oscillator including:

a primary current source coupled to the control input;

a differential switch coupled to the primary current source;

a capacitor coupled to the differential switch; and

a comparator coupled to the differential switch;

a digital to analog converter coupled to the control input, the [analog to] digital to analog converter having one or more current sources, wherein the primary current source generates a current I and each of [the] said one or more current sources generates a current lower than I;

a counter coupled to the output of the oscillator and to the current sources of the digital to analog converter; and

a power transistor coupled to the oscillator and to one terminal of the primary winding, the power transistor modulating its output in providing a regulated power supply output.

<sup>32</sup>

<sup>34</sup> (Amended) A power supply having a transformer coupled to an input voltage, the transformer having a primary winding, the power supply comprising:

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an oscillator for generating a signal having a frequency, the oscillator having a control input for varying the frequency of the signal, the oscillator including:

a primary current source coupled to the control input;

a differential switch coupled to the primary current source;

a capacitor coupled to the differential switch; and

a comparator coupled to the differential switch

a circuit for varying the frequency, the circuit coupled to the control input, including:

a capacitor;

a current source adapted to charge and discharge the capacitor;

one or more comparators coupled to the capacitor and coupled to the current

source for alternately charging and discharging the capacitor; and

a power transistor coupled to the oscillator and to one terminal of the primary winding,

the power transistor modulating its output in providing a regulated power supply output.

#### REMARKS

Claims pending in the instant application are numbered 1-34. Claims 11-34 presently stand rejected. The Applicants note with appreciation that claims 1-10 presently stand allowed. The title and claims 11, 17, 21, 23, 26-28, 30, 32, 33 and 34 have been amended. The Applicants respectfully request reconsideration of the present application as amended.

#### *Title Objection*

In the October 16, 2000 Office Action, the title of the invention is objected to as being imprecise. The Applicants have amended the title as suggested by the Examiner.

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*35 USC § 112 Rejections of Claims*

In the October 16, 2000 Office Action, claims 27-28 and 32-34 are rejected under 35 USC § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the Applicant regards as the invention. The Applicants have amended claims 27, 28, 32, 33 and 34 and the instant section 112 rejections have been overcome. The Applicants respectfully request withdrawal of the instant section 112 rejections.

*35 USC § 102 Rejections of Claims*

In the October 16, 2000 Office Action, claims 11, 13, 17, 21 and 31-32 are rejected under 35 USC § 102(b) as being anticipated by Albach, US Patent No. 4,712, 169.

Claim 11 as presently amended presently recites "*combining the secondary current with the primary current to be received at a control input of an oscillator . . .*" To illustrate, attention is respectfully directed to the example embodiment illustrated in Figure 1. The secondary current from current sources 152, 156, 160 and 164 are *combined* with the primary current 125 to be received at the control input node 123 of the oscillator. (See, e.g., page 14, lines 14-20 of the Applicants' specification).

In contrast, Albach fails to disclose teach or suggest *combining* a secondary current with a primary current *to be received at a control input of an oscillator*. Instead, Albach suggests a reference voltage  $U_{ref}$  that is received at a positive input of a comparator 31 and a voltage  $U_1$  that varies over time that is received at a negative input of comparator 31. Albach fails to disclose teach or suggest that  $U_1$  is combined with  $U_{ref}$  and is received at a control input  $U_2$  of VCO 34. Indeed, Albach fails to disclose teach or suggest that  $U_{ref}$  and  $U_1$  are added together to form  $U_2$ . Accordingly, Albach

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fails to disclose, teach or suggest expressly recited elements of claim 11 as presently amended.

Claim 17 distinguishes for the same reasons described above in connection with claim 11.

Claim 21 has been amended to embody limitations included in conditionally allowed claim 22. The Applicants understand claim 21 should be allowable as amended in view of the Examiner's indication of allowable subject matter in paragraph 10 of the October 16, 2000 Office Action.

Claims 13, 31 and 32 are dependent claims and therefore distinguish for at least the same reasons as their respective independent base claims in addition to adding further limitations of their own.

Accordingly, the Applicants respectfully submit that instant section 102 rejections have been overcome and request withdrawal of the instant section 102 rejections.

*35 USC § 103 Rejections of Claims*

In the October 16, 2000 Office Action, claims 12 and 18 are rejected under 35 USC § 103 as being obvious in view of Albach. Claims 12 and 18 are dependent claims and therefore distinguish for at least the same reasons as their respective independent base claims in addition to adding further limitations of their own. Accordingly, the Applicants respectfully request withdrawal of the instant section 103 rejections

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Examiner: D. Butler  
Art Unit: 2182

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**Charge Deposit Account**

Please charge our Deposit Account No. 02-2666 for any additional fee due in this matter.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

Date:

1/8/01

James Y. Go  
Reg. No. 40,621

**FIRST CLASS CERTIFICATE OF MAILING**

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on

January 8, 2001

Date of Deposit

Melanie Resecker

Name of Person Mailing Correspondence

Melanie Resecker

Signature

Date

1-8-01

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Serial No. 09/192,959

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Examiner: D. Butler  
Art Unit: 2182

FCS0000097

**8**

**FCS0000098**



UNITED STATES DEPARTMENT OF COMMERCE  
Patent and Trademark Office  
Address: COMMISSIONER OF PATENTS AND TRADEMARKS  
Washington, D.C. 20231

APPLICATION NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.
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09/192,959 11/16/98 BALAKRISHNAN

EXAMINER 10256/003001

TM01/0130

BRADLEY J. BEREZNAK, ESQ.  
BLAKELY SOKOLOFF TAYLOR & ZAFMAN, LLP  
12400 WILSHIRE BLVD.  
SEVENTH FLOOR  
LOS ANGELES CA 90025

ART UNIT 1 PAPER NUMBER 8

DATE MAILED: 82

01/30/01

This is a communication from the examiner in charge of your application.  
COMMISSIONER OF PATENTS AND TRADEMARKS

#### NOTICE OF ALLOWABILITY

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance and Issue Fee Due or other appropriate communication will be mailed in due course.

☒ This communication is responsive to amendment A

☒ The allowed claim(s) is/are 1-21, 23-28 and 30-34

☐ The drawings filed on \_\_\_\_\_ are acceptable.

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) \_\_\_\_\_

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

\*Certified copies not received: \_\_\_\_\_

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

A SHORTENED STATUTORY PERIOD FOR RESPONSE to comply with the requirements noted below is set to EXPIRE THREE MONTHS FROM THE "DATE MAILED" of this Office action. Failure to timely comply will result in ABANDONMENT of this application. Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

☐ Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL APPLICATION, PTO-152, which discloses that the oath or declaration is deficient. A SUBSTITUTE OATH OR DECLARATION IS REQUIRED.

☒ Applicant MUST submit NEW FORMAL DRAWINGS

☐ because the originally filed drawings were declared by applicant to be informal.

☒ including changes required by the Notice of Draftsperson's Patent Drawing Review, PTO-948, attached hereto or to Paper No. 6

☐ including changes required by the proposed drawing correction filed on \_\_\_\_\_, which has been approved by the examiner.

☐ including changes required by the attached Examiner's Amendment/Comment.

Identifying indicia such as the application number (see 37 CFR 1.54(c)) should be written on the reverse side of the drawings. The drawings should be filed as a separate paper with a transmittal letter addressed to the Official Draftsperson.

☐ Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Any response to this letter should include, in the upper right hand corner, the APPLICATION NUMBER (SERIES CODE/SERIAL NUMBER). If applicant has received a Notice of Allowance and Issue Fee Due, the ISSUE BATCH NUMBER and DATE of the NOTICE OF ALLOWANCE should also be included.

Attachment(s)

☐ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s) \_\_\_\_\_

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

☐ Interview Summary, PTO-413

☐ Examiner's Amendment/Comment

☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material

☐ Examiner's Statement of Reasons for Allowance

*Dennis M. Butler*

Dennis M. Butler  
Primary Examiner

*SM*

PTOL-37 (Rev. 10/95)

U.S. GPO: 1997-417-381/62714

FCS0000099



UNITED STATES DEPARTMENT OF COMMERCE  
Patent and Trademark Office

**NOTICE OF ALLOWANCE AND ISSUE FEE DUE**

TN01/0129

BRADLEY J. BEREZNAK, ESQ.  
BLAKELY SOKOLOFF TAYLOR & ZAFMAN, LLP  
12400 WILSHIRE BLVD.  
SEVENTH FLOOR  
LOS ANGELES CA 90025

APPLICATION NO.	FILED DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT	DATE MAILED
09/192,959	11/16/98	032	BUTLER, D	2182 01/30/01
First Named Applicant	BALAKRISHNAN,	35 USC 154(b) term ext. =	0 Days.	

TITLE OF INVENTION: FREQUENCY JITTERING CONTROL FOR VARYING THE SWITCHING FREQUENCY OF A POWER SUPPLY

ATTY'S DOCKET NO.	CLASS-SUBCLASS	BATCH NO.	APPL. TYPE	SMALL ENTITY	FEE DUE	DATE DUE
0	10256/003001	713-501.000	B25 UTILITY	NO	\$1240.00	04/30/01

**THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED.**

**THE ISSUE FEE MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED.**

**HOW TO RESPOND TO THIS NOTICE:**

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

- A. If the status is changed, pay twice the amount of the FEE DUE shown above and notify the Patent and Trademark Office of the change in status, or
- B. If the status is the same, pay the FEE DUE shown above.

If the SMALL ENTITY is shown as NO:

- A. Pay FEE DUE shown above, or
- B. File verified statement of Small Entity Status before, or with, payment of 1/2 the FEE DUE shown above.

II. Part B-Issue Fee Transmittal should be completed and returned to the Patent and Trademark Office (PTO) with your ISSUE FEE. Even if the ISSUE FEE has already been paid by charge to deposit account, Part B Issue Fee Transmittal should be completed and returned. If you are charging the ISSUE FEE to your deposit account, section "4b" of Part B-Issue Fee Transmittal should be completed and an extra copy of the form should be submitted.

III. All communications regarding this application must give application number and batch number. Please direct all communications prior to issuance to Box ISSUE-FEE unless advised to the contrary.

**IMPORTANT REMINDER: Utility patents (issuing on applications filed on or after Dec. 12, 1980) may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.**

**PATENT AND TRADEMARK OFFICE COPY**

PTOL-45 (REV. 10-98) Approved for use through 06/30/99. (P031-0033)

FCS0000100







Docket No.: 005510.P033 <sup>B</sup>

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE <sup>#9MK</sup>

In re Application for:

Balu Balakrishnan et al.

Application No.: 09/192,959

Filed: November 16, 1998

For: FREQUENCY JITTERING CONTROL FOR  
VARYING THE SWITCHING FREQUENCY  
OF A POWER SUPPLY

Examiner: D. Butler

Art Group: 2182

Batch No: B25

TRANSMITTAL OF FORMAL DRAWINGS

Attn: Official Draftsman  
Assistant Commissioner for Patents  
Washington, D.C. 20231

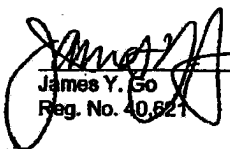
Dear Sir:

Enclosed herewith for filing in the above-identified U.S. patent application are the  
formal drawings, Figures 1, 2, 3, 4, 5 and 6 (6) sheets.

Respectfully submitted,


BLAKELY SOKOLOFF TAYLOR & ZAFMAN, LLP

Date: 4-24-01

  
James Y. Go  
Reg. No. 40,821

12400 Wilshire Boulevard  
Seventh Floor  
Los Angeles, CA 90025  
(425) 827-8600

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April 24, 2001

  
Rimma N. Oks  
typed or printed name of person making correspondence  
04/24/01  
Date

01/01

FCS0000102

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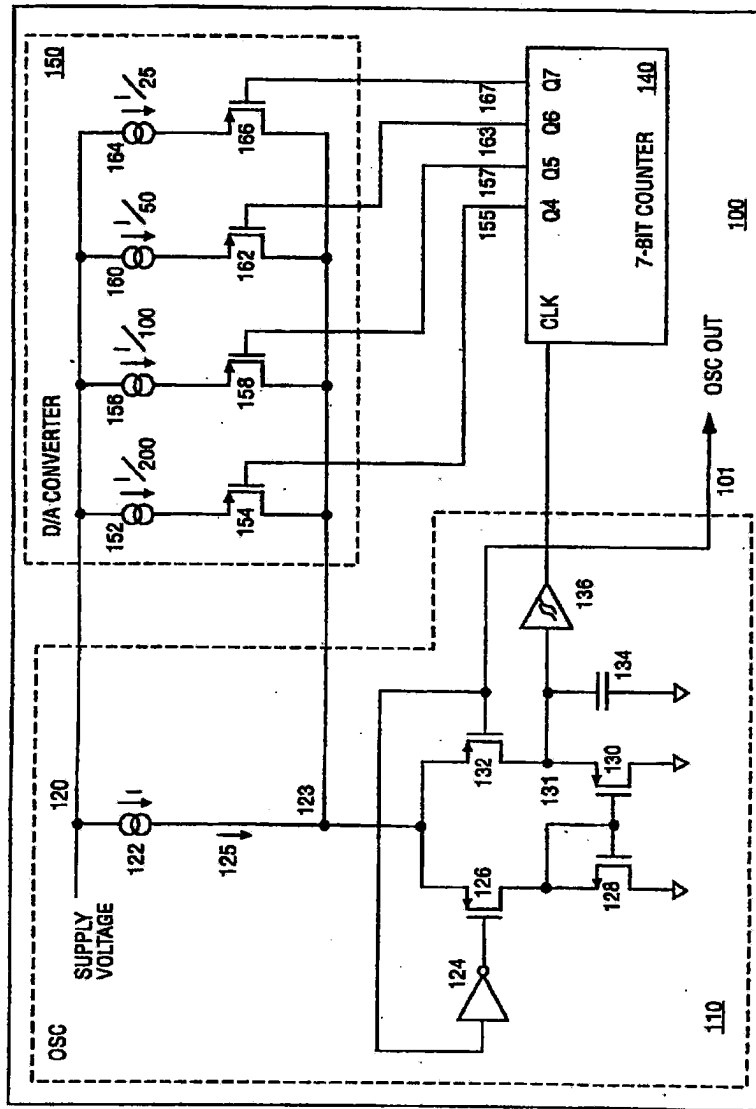


FIG. 1

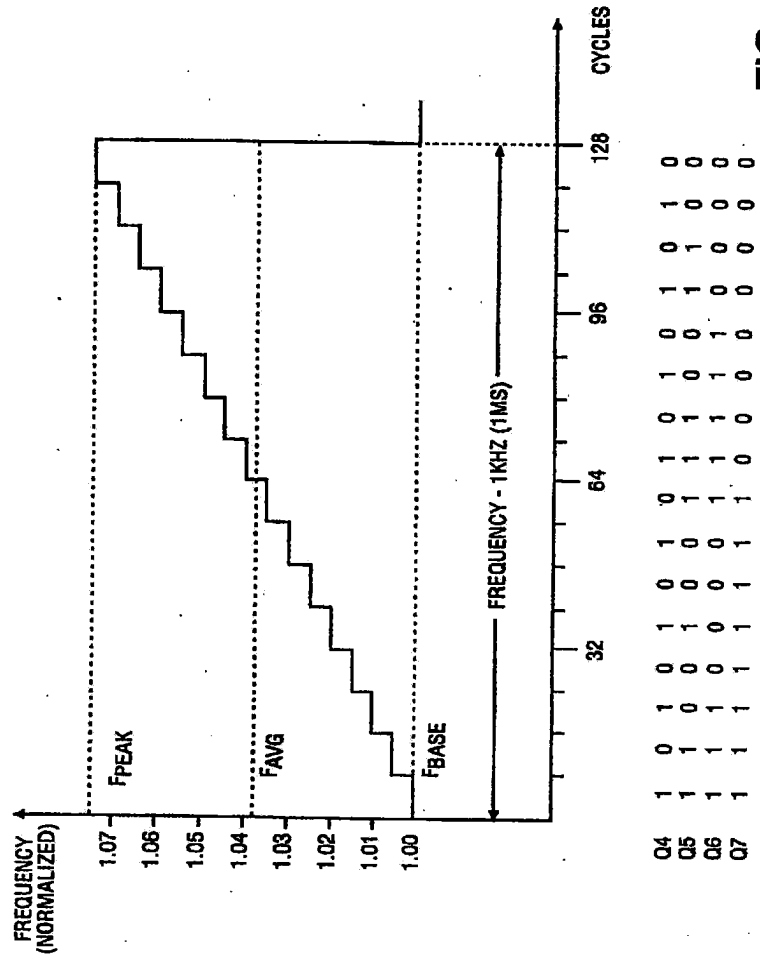


FIG. 2

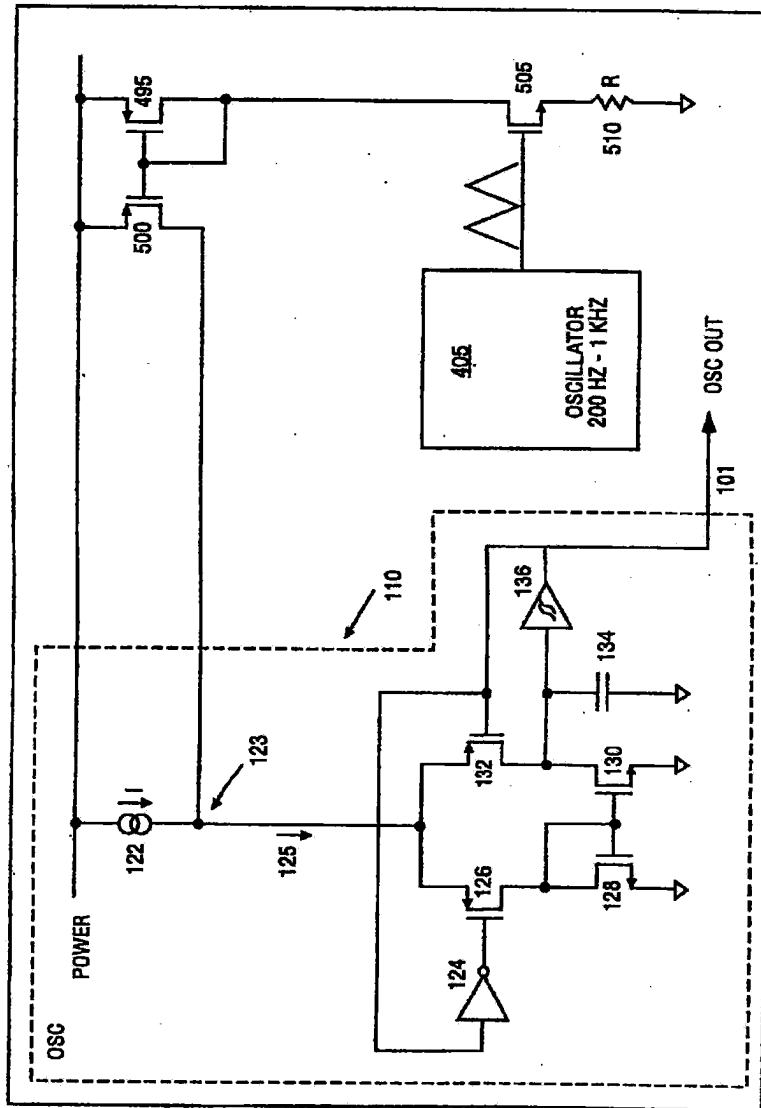


FIG. 3

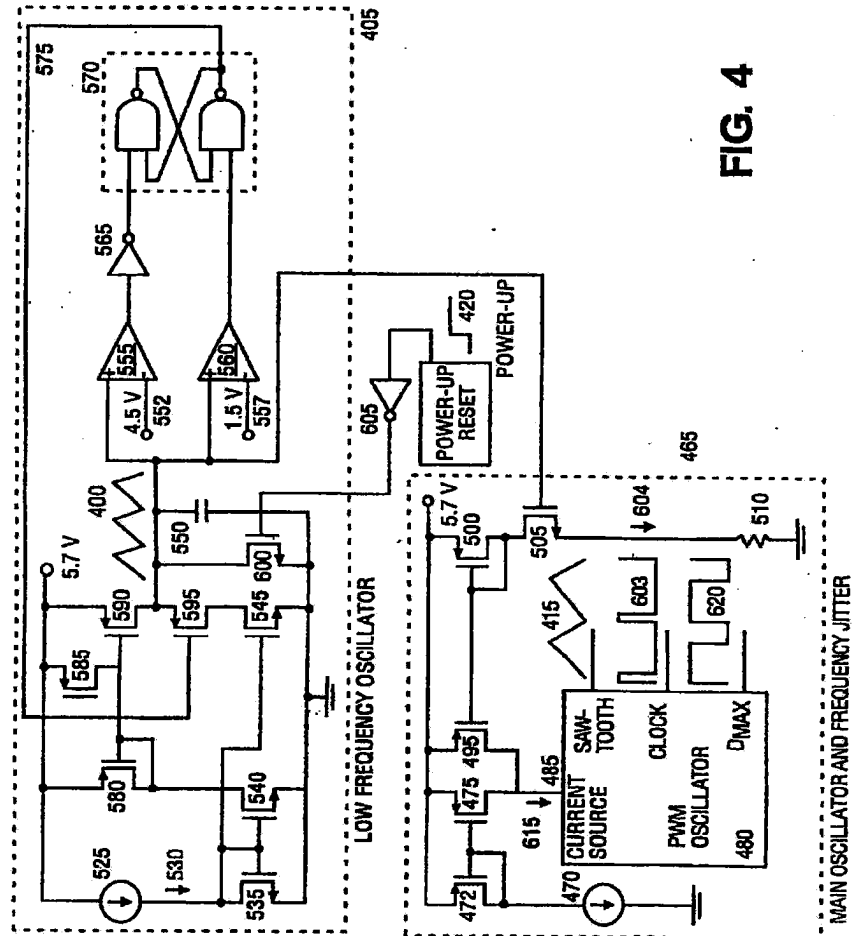


FIG. 4

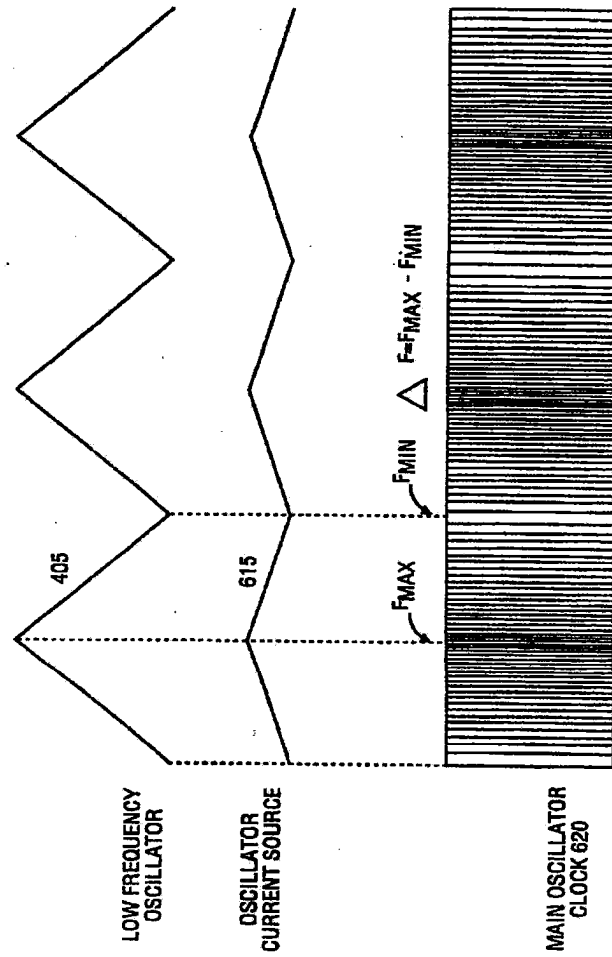
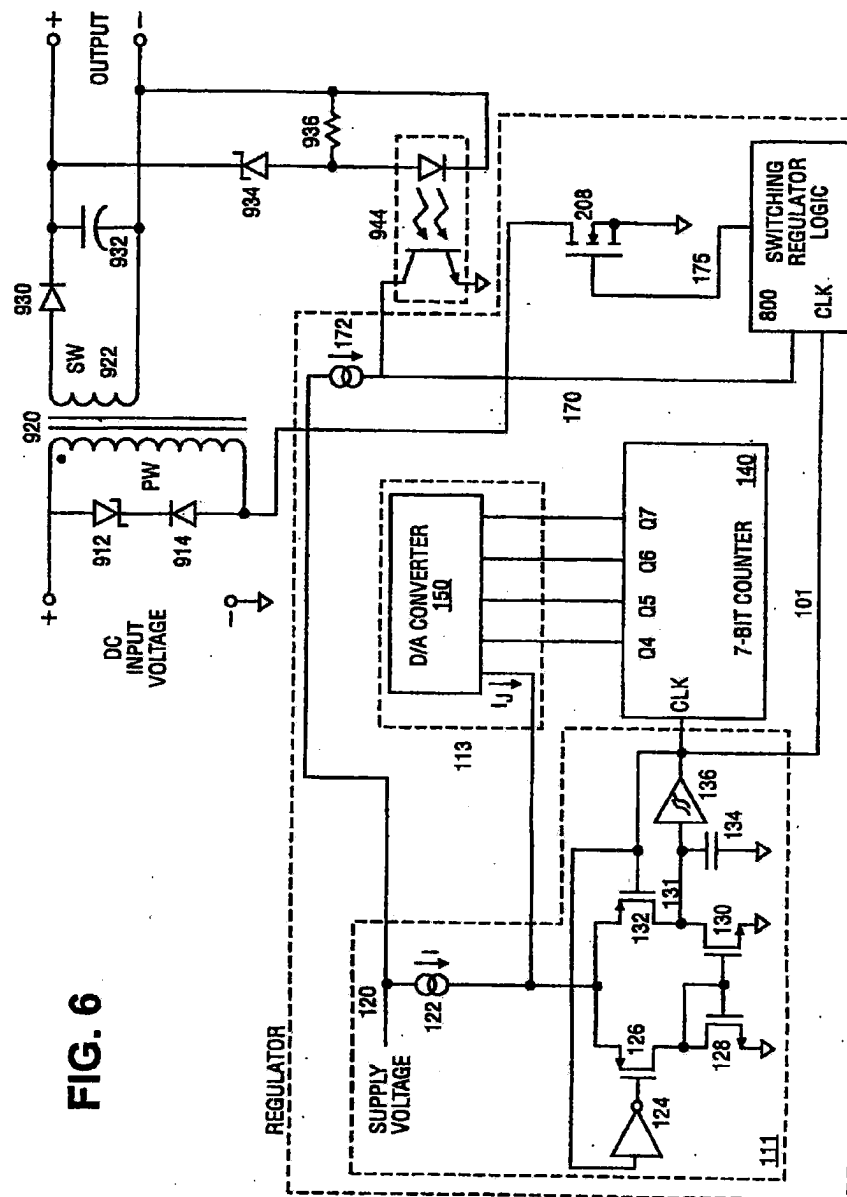


FIG. 5

**FIG. 6**



Bc

**PART 2 - ISSUE FEE TRANSMITTAL**

Complete this form, together with applicable fees, to: **Box ISSUE FEE**  
Assistant Commissioner for Patents  
Washington, D.C. 20231

**MAIL INSTRUCTIONS:** This form should be used for transmitting the ISSUE FEE. Blocks 1 through 4 should be completed where appropriate. All further correspondence including the Issue Fee Receipt, the correspondence orders and notification of maintenance fees will be mailed to the client correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

**CURRENT CORRESPONDENCE ADDRESS** (Note: Lightly mark up with any corrections or use Block 1)

TM01/0129

**BRADLEY J. BEREZNAK, ESQ.**  
**BLAKELY SOKOLOFF TAYLOR & ZAFMAN, LLP**  
**12400 WILSHIRE BLVD.**  
**SEVENTH FLOOR**  
**LOS ANGELES CA 90025**

**Block 1** (Note: The certificate of mailing below can only be used for domestic mailings of the Issue Fee Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing.)

**Certificate of Mailing**

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**Block 3** (Date)

**Block 4** (Time)

APPLICATION NO.	FILING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT	DATE MAILED
09/192,959	11/16/98	032	BUTLER, D	2182 01/30/01

**First Named Applicant** **BALAKRISHNAN,** **35 USC 154(b) term ext. = 0 Days.**

**TITLE OF INVENTION** **FREQUENCY JITTERING CONTROL FOR VARYING THE SWITCHING FREQUENCY OF A POWER SUPPLY**

ATTY'S DOCKET NO.	CLASS-SUBCLASS	BATCH NO.	APPL. TYPE	SMALL ENTITY	FEE DUE	DATE DUE
0	10256/003001	713-601.000	B25 UTILITY	NO	\$1240.00	04/30/01

1. Change of correspondence address or indication of "Fee Address" (PT CPH 1.203). Use of PTO form(s) and Customer Number are recommended, but not required.

☐ Change of correspondence address (for Change of Correspondence Address form PTO/SB47) attached.

☐ "Fee Address" indication (or "Fee Address" indication form PTO/SB47) attached.

2. For printing on the patent front page, list (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, (2) the name of a single firm (having at a member a registered attorney or agent) and the names of up to 3 registered patent attorneys or agents. If no name is listed, no name will be printed.

**BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, LLP.**

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

**PLEASE NOTE:** Unless an assignee is identified below, no assignee data will appear on the patent. Indication of assignee data is only appropriate when an assignment has been previously submitted to the PTO or is being submitted under separate cover. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE **Power Integrations, Inc.**

(B) RESIDENCE: (CITY A STATE OR COUNTRY) **San Jose, California**

Please check the appropriate assignee category indicated below (full not to be printed on the patent)

☐ Individual ☒ corporation or other private group entity ☐ government

4a. The following fees are enclosed (make check payable to Commissioner of Patents and Trademarks):

☒ Issue Fee

☐ Advance Order - # of Copies **10**

4b. The following fees or deficiency in these fees should be charged to:

DEPOSIT ACCOUNT NUMBER **02-2666**  
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☒ Issue Fee

☐ Advance Order - # of Copies **10**

The COMMISSIONER OF PATENTS AND TRADEMARKS IS requested to apply the Issue Fee to the application identified above.

(Authorized Signature) **James Y. Co** (Date) **04-26-01**

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**Block 6** (Date)

**Block 7** (Time)

**Block 8** (Time)

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**Block 10** (Time)

**Block 11** (Time)

**Block 12** (Time)

**Block 13** (Time)

**Block 14** (Time)

**Block 15** (Time)

**Block 16** (Time)

**Block 17** (Time)

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DENVER / ENGLEWOOD, CO



July 16, 2001

**REVIEW**

**APPROVED**

JAN 30 2002  
FOR THE DIRECTOR OF USPTO

Hon. Commissioner of Patents  
and Trademarks  
Washington, D.C. 20213

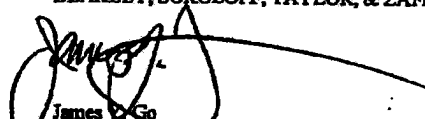
Re: **CERTIFICATE OF CORRECTION**  
U.S. Letters Patent No. US 6,249,876 B1  
Issued: June 19, 2001  
For: **FREQUENCY JITTERING CONTROL FOR VARYING THE  
SWITCHING FREQUENCY OF A POWER SUPPLY**  
Inventor: Balakrishnan et al.  
Our File No.: 005510.P033

Dear Sir:

Enclosed is a Certificate of Correction (two copies) for the above-referenced patent.

This request for correction is made under rule 322 of the Rules of Practice and 35 U.S.C. Section 254.

Respectfully submitted,  
BLAKELY, SOKOLOFF, TAYLOR, & ZAFMAN LLP

  
James L. Go  
Reg. No. 40,621

**CERTIFICATE**  
JUL 19 2001  
**OF CORRECTION**

JYG/jem  
enclosures

FCS0000111

**UNITED STATES PATENT AND TRADEMARK OFFICE  
CERTIFICATE OF CORRECTION**

**PATENT NO. :** US 6,249,876 B1

**DATED :** June 19, 2001

**INVENTOR(S) :** Balakrishnan et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 10, line 2, please insert -- current -- after "primary".

Column 10, line 3, please delete "wherein the oscillator further" and insert -- wherein the differential switch further --.

**MAILING ADDRESS OF SENDER:**  
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP  
12400 Wilshire Blvd. 7th floor  
Los Angeles, CA 90025-1026

**PATENT NO. US 6,249,876 B1**

**Certificate of Correction (PTO Form 1050)-Amended**

n/a

FCS0000112

**UNITED STATES PATENT AND TRADEMARK OFFICE  
CERTIFICATE OF CORRECTION**

**PATENT NO. :** US 6,249,876 B1

**DATED :** June 19, 2001

**INVENTOR(S) :** Balakrishnan et al.

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12400 Wilshire Blvd. 7th floor  
Los Angeles, CA 90025-1026

**PATENT NO. US 6,249,876 B1**

**Certificate of Correction (PTO Form 1050)-Amended**

n/a

FCS0000113

UNITED STATES PATENT AND TRADEMARK OFFICE  
CERTIFICATE OF CORRECTION

PATENT NO. : 6,249,876 B1  
DATED : June 19, 2001  
INVENTOR(S) : Balakrishnan et al.

Page 1 of 1

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 10.

Line 2, please insert -- current -- after "primary".

Line 3, please delete "wherein the oscillator further" and insert -- wherein the differential switch further --.

Signed and Sealed this

Nineteenth Day of February, 2002

Attest:



Attesting Officer

JAMES E. ROGAN  
Director of the United States Patent and Trademark Office

FCS0000114